

A D V A N C I N G

# MICROELECTRONICS

EVERYTHING IN ELECTRONICS BETWEEN THE CHIP AND THE SYSTEM!

JULY/AUGUST 2008

Vol. 35 No. 4

## Materials and Thermal Management

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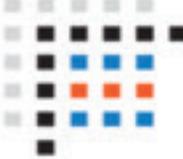
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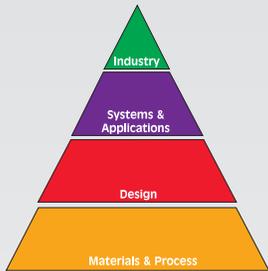
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August 12-14, 2008 Albuquerque, NM

## ATW on RF and Microwave Packaging

September 16-18, 2008 San Diego, CA

## XXXII International Microelectronics and Packaging IMAPS-CPMT Poland

September 22-23, 2008 Pultusk, Poland

## Advanced Technology Workshop on Thermal Management

October 14-16, 2008 Palo Alto, California

## 7th International Symposium on Microelectronics and Packaging (ISMP 2008)

October 15-17, 2008 Seoul, Korea

## IMAPS 2008

November 2-6, 2008 Providence, RI

## Emerging Microelectronics and Interconnection Technology (EMIT 2008)

December 15-18, 2008 Bangalore, India

## ATW and Tabletop Exhibit on Printed Devices and Applications

February 25-27, 2009 Orlando, FL

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Steven J. Adamson,  
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## Our Purpose and How We Are Organized

This year IMAPS celebrated its fortieth anniversary. In all of these years our members have been sharing ideas and educating the next generation. This role keeps expanding as new technologies come along and we have to adapt the society to meet the new challenges. IMAPS has been from its inception a loosely organized group. Our chapters are very independent and that frees them to be responsive to local requirements; no one is telling them what programs they need to put on or how to do it. If they want they can ask for help from the International Head Quarters (IHQ) staff. This arrangement extends beyond the shores of the USA, all chapters are equal. The IHQ staff are there to facilitate organization of events and publishing *Advancing Microelectronics*. They maintain the web pages and fulfill many functions that volunteers do not have the time to take on, such as booking hotels and meeting rooms for international conferences and meetings. This ever-evolving organization with its loose ties has grown to the largest Microelectronic Packaging society in the world, several times larger than IEEE-CPMT. It would appear that the model has been very successful.

Recently there was a proposal to change the way the society is organized. Some people felt that our Executive Council (EC) was dominated by the US members. This is true, our EC has been composed of members from the US, although we have had one past president who came from the UK. Members drive the composition of the Executive Council. Typically, it is US members who participate in the leadership of IMAPS functions so they become known to the membership and are as a consequence nominated and elected. It was proposed that we form an international governing council, similar to how the United Nations operates. This would allow our non-US affiliates a greater say in how the society is run. The IMAPS executive asked for guidance on this subject from the Advisory committee. The Advisory Committee is composed of the society's past presidents; they form the corporate memory of the society. The one striking response from them was the fact that the society was set up to be a loosely organized group, and they did not want to have strong upper level management of the society at its inception. Further feedback suggested that if we did make changes we should not increase costs to the member. So based on this feedback the EC reviewed the proposed suggestions and voted not to make any changes to the way the society is organized. This was reported to the World Liaison Committee (WLC) in Munich this past April, by Mike Ehlert. The WLC is a group formed

to allow IMAPS chapters from around the world to have informal discussions and coordinate calendars, etc. It is not a governance function.

One thing to remember here is that there is an "I" in IMAPS, we currently have an international body. Members from any country can run in the elections for EC positions. There are no set asides for members from any region, we do not discriminate or favor people from any region or for any reason.

We have one golden rule in IMAPS. A member is a member, no matter where they are from. How do we know you are a member? We know you are a member because you have registered as a member and paid dues. In some parts of the world the IMAPS chapters have local members. They pay dues to the local chapter but nothing is sent to the HQ. As well as Regular Membership we also have International Affiliate membership. These are IMAPS members too and are entitled to all the benefits of membership, including running in elections for the EC. This addresses some of the economic differences around the world. Some of the international chapters have complained that members should not have to pay the local chapter and send money to the US for an International Affiliate membership. Unfortunately these days, if we want to run a lean staff and control costs, we have to depend on our computers to do some of the work for us. If a person outside of the US is not willing to support IMAPS by paying for the Affiliate membership which currently is set at \$20, we cannot afford to send them copies of *Advancing Microelectronics* or let them into our member sites on the web or offer them member discounts at IMAPS events and the other benefits of IMAPS membership.

We have one golden rule, a Member is a Member is a Member, but you have to demonstrate that you want to be a member by paying membership dues either as a full or international affiliate member. This also gets you a vote at the next election.

We want our chapters to be successful, we want the European and Asian members of IMAPS to go out and build the society in the areas we have not operated previously. International Headquarters will gladly support their efforts.

We are organized on a very loose basis with no large central bureaucracy; we have many geographically separated independent chapters. We are organized to be flexible and therefore can be entrepreneurial. Let's keep our education mission in front of us, to help the next generation and share ideas to help us be better at what we do.

# Materials and Thermal Management: Challenges on All Fronts

The July / August issue of *Advancing Microelectronics* covers two topics that come up everywhere in the industry – materials and thermal management.

Incidents of overheated electronics make mainstream news, and entire product lines have been revamped to reduce power, to the point where low power is now a critical differentiator in the marketplace for many types of ICs. An informal survey of advertisements in a chip industry publication showed a surprisingly high fraction highlighting power reduction or power management, rather than advanced silicon technology or some new kind of functionality. Dealing with the heat generated by semiconductors is a huge challenge – but one that is squarely in the scope of IMAPS. Whether it is conductive materials, packaging, heatsinking, or system-level solutions, many players in the industry can contribute to thermal solutions.

Similarly, there are widespread challenges in materials these days everywhere in the semiconductor industry. Adhesives, coatings, interconnect materials, substrates, dielectrics ... the list of critical types of materials in the semiconductor industry is very long. Roadmaps such as the ITRS and iNEMI's publications highlight materials issues as some of the biggest hurdles facing the industry. Again, the scope of IMAPS covers this thoroughly. In fact, many of the traditional, long-term IMAPS members are materials companies, and we are glad to contribute to progress in the industry at its foundation.

At the industry level, we are glad to have an article by Dan Tracy of SEMI, who reviews packaging material market trends, including the cost of gold wire and the issue of the ROI on materials R&D. Diving deep into the technology, Jonathan Harris and Erich Rubel of CMC Interconnect Technology discuss the reliability effects of interfacial compounds. As a (former?) material scientist, I appreciate the detail and thoroughness of their work on this important topic.

A team from Reactive NanoTechnologies provided a nice article about their novel technology that produces localized heat for a variety of applications. In this case, it provides room temperature soldering for attachment of high power components. Finally, EPCOS in Germany wrote about thermal management of flip chip assemblies in LTCC, which is certainly an important and complex challenge.

We thank our authors for contributing to another issue that we think should be of great interest to our members.

Oh, and don't forget to carve out some time on your calendar for the IMAPS 41<sup>st</sup> International Symposium on Microelectronics coming up, back on the East Coast this year – Providence, RI, November 2 – 6, 2008. November isn't as far away as you think. Time flies when you're having fun ... which certainly applies to those of you having fun addressing critical challenges in materials and thermal management!

Thanks for reading,  
Jeff Demmin



Jeff Demmin, Tessera Technologies, Inc., Editor-in-Chief

## OOPS!

In the last issue, we misspelled two names in the Nordson Student Award article.

Participants in the photo are Dr. Len Schaper, University of Arkansas, Student Advisor to the winner, Ying Mao (the student winner's wife), Michael O'Donoghue, the winner of the award to Mr. Yang Liu (University of Arkansas) and Ray McHenry of Nordson Corp. The location is the Device Packaging Conference of IMAPS, [www.imaps.org](http://www.imaps.org), a highly successful event with over 650 attendees.



Søren Nørlyng, Micronsult,  
noerlyng@micronsult.dk

## The European Way

To demonstrate the *International* aspect in IMAPS the well established CICMT (Ceramic Interconnect and Ceramic Microsystems Technologies) event which has taken place in Denver moved to Europe this year and is planned to move to Japan 2010.

Ceramic technologies have still a very high focus in Europe (and Japan) for use in automotive electronics and even mobile phone front end modules – besides in numerous RF and sensor applications. What could be more natural than to take the event to where the expertise and interest is seen.

The initiative came from individuals in IMAPS Germany and together with the German Ceramic Society with IMAPS NA and the American Ceramic Society as cosponsors the conference moved to Munich. The local arrangement – and work – was now on the shoulders of the German team.

The conference was a success. More than 250 delegates and 31 exhibitors enjoyed the 2.5 day event with 75 oral presentations and 50 poster presentations.

The European touch was clearly seen in the generous provisioning and hospitality arrangements. The (south) German touch was seen in the abundance of food, beer and wine. All arrangements except the conference dinner took place in the exhibition area, so definitely all exhibitors were exposed and busy during the conference days.

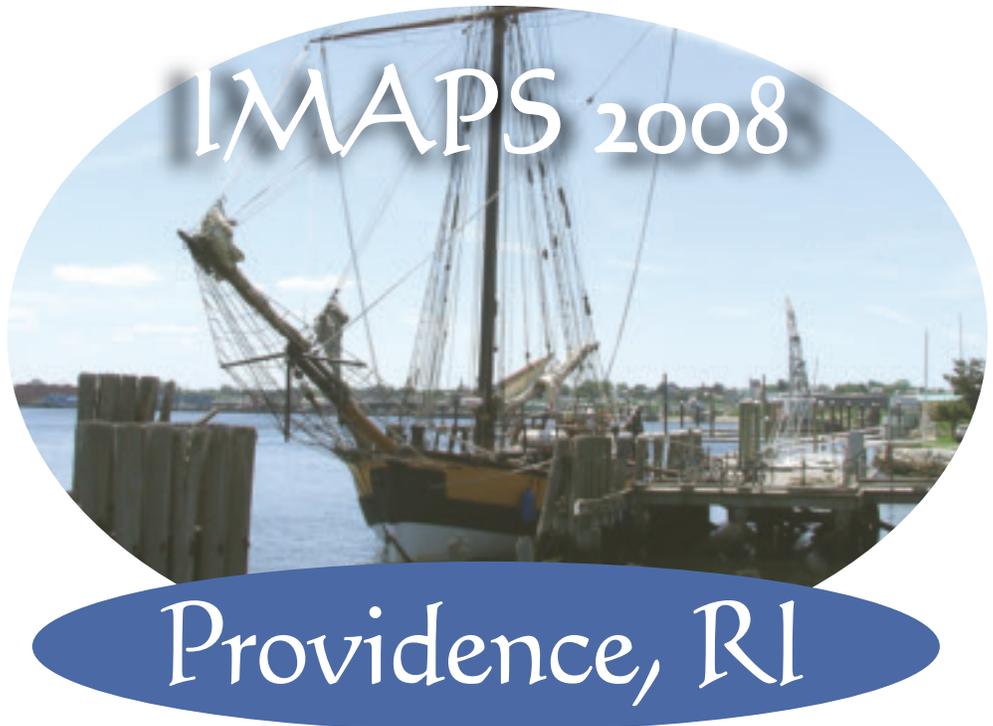
The conference dinner took place in a beer cellar and several IMAPS Germany traditions could be enjoyed: hammering the drain cock into the beer barrel(s) without emptying the beer on the floor or on your clothes, and the traditional Bavarian dishes.

Definitely a conference you will remember – not only for its excellent technical program – but also for the many new people you had time to meet due to the very social ambience perfect for networking opportunities. Many thanks to our hosts!

Søren Nørlyng  
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*The conference  
was a success.*

*More than 250 delegates  
and 31 exhibitors ...*



[www.imaps2008.org](http://www.imaps2008.org)

# Call for Technical Manuscripts

We invite all individuals involved in related technologies to submit manuscripts for the *Journal of Microelectronics and Electronic Packaging*.

The IMAPS Journal is a prestigious, refereed, and archival publication distributed worldwide to IMAPS members, educational institutions, and corporate libraries. Complete information regarding this publication may be found on the IMAPS website at [www.imaps.org](http://www.imaps.org); however, the key points are:

- All submissions must be in electronic format, and should be submitted via EMail to [jmep@imaps.org](mailto:jmep@imaps.org).
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- Papers should preferably be written in Microsoft Word.
- Tables, graphs, and photographs should be submitted at the end of the file and need not be embedded in the text.
- Photographs and other illustrations should preferably be submitted in JPEG, GIF or WMF format.

**Authors of papers that have been printed in other IMAPS publications or presented at IMAPS workshops are invited to submit updated and/or expanded versions of their papers for possible publication in the Journal.**

We invite your suggestions on how to improve the Journal in any way. Please send all submissions, comments, or questions to [jmep@imaps.org](mailto:jmep@imaps.org).

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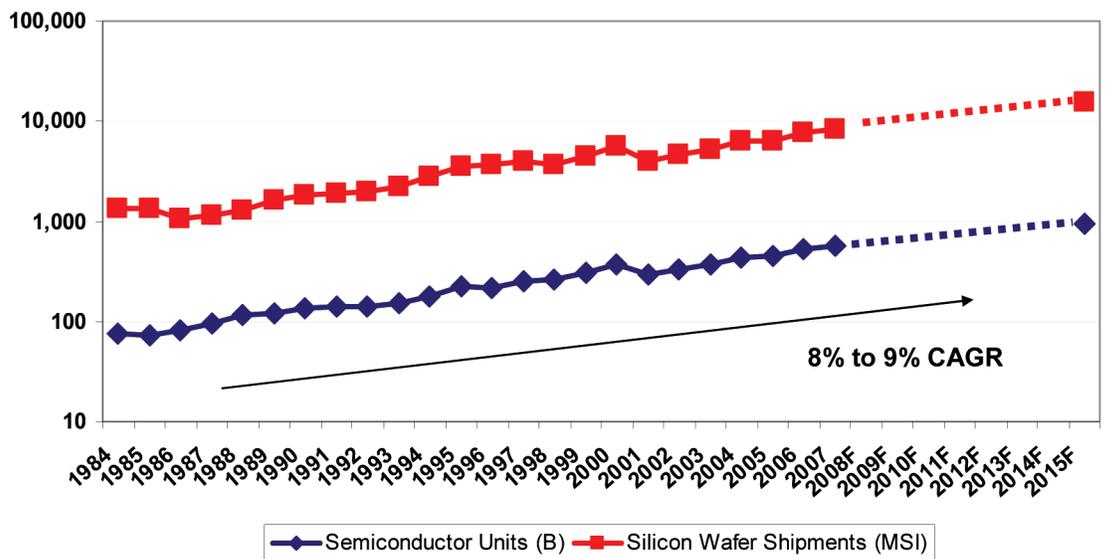
# Semiconductor Material Market Trends

Dan Tracy, Senior Director Industry Research & Statistics, SEMI

A positive trend for suppliers of semiconductor materials, including both the fab and packaging segments of the industry, is that demand for semiconductor devices will continue to increase as electronic products become ever more widespread in our lives. This demand growth for semiconductor devices means that wafers, chemicals, resins, solder, and other materials are consumed in the fabrication and assembly of each device.

The accompanying figure shows the history of both semiconductor device unit sales and silicon wafer shipments over the past 24 years. As expected, the correlation between the two is strong, with both growing at 8% to 9% compound annual growth rate (CAGR) trend over this time period. Making a simple assumption that this 8% to 9% trend growth can be maintained through the middle of the next decade, we are looking at an industry that could consume 15 billion square inches or so of silicon to produce 900 billion devices.

Semiconductor and Silicon Unit Shipments



Source: WSTS, Rose Associates, and SEMI

Over time, the semiconductor industry has become more efficient in processing materials and in the amount consumed in both wafer fabrication and package assembly. Layers and structures on the chip are becoming thinner and finer in size, and many packaging form factors are thinner and smaller with, in some cases, multiple die stacked inside a single package. Technical challenges abound for suppliers as the industry advances device scaling and systems integration to increase device performance. Key to these innovations are materials. Declining dimensions of films and device structures are pushing the limits to our current understanding of interfacial interactions and surface effects. Each generation of device technology is becoming more

and more complex with respect to process integration. Specific to packaging, where new and complicated form factors are being developed, new materials are needed to assemble reliable devices that have increased functionality.

Beyond technology, two economic challenges stand front and center of the semiconductor industry regarding material technology development and consumption.

First is the recent trend in rising commodity prices for various raw and starting materials. Specific to packaging are the rising costs of important materials: resins, copper, tin, gold, silver, and palladium. There has been a sharp rise in pricing for these materials over the past

several years and, as a result, this has spurred development efforts either to reduce the amount of metal consumed or, in some cases, investigate replacement materials. For companies assembling packages, the challenge is that some of the advanced packaging technologies, such as CSP and wire bond Ball Grid Arrays (BGA), are viewed as commodity technologies, so higher material costs are detrimental in achieving acceptable margins.

A prime example is the price of gold, which was \$400 per troy ounce four years ago, and in the past quarter briefly reached over \$1,000 per troy ounce. (By late April/early May 2008, the average daily price declined to under \$900 per troy ounce.) Gold wire is used for all types of packaging applications and it represents more than 90% of the worldwide bonding wire market in both volume and, of course, value. Reportedly, pricing of the high purity gold metal represents an estimated 85% of the total cost of 25 micron diameter wire.

The impact of the rising cost of gold has compelled manufacturers to migrate towards smaller diameter wire where appropriate and look at alternative technologies:

- The majority of the gold wire market now consists of 25 micron or less diameter wire.
- Suppliers are increasing wire spool lengths to help control costs through improved set up times and production yields at assembly.
- Higher gold pricing has contributed to the interest and on-going development in copper bonding wire.

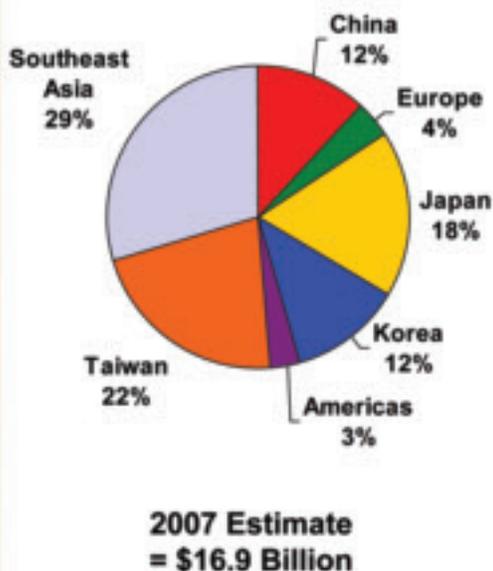
Copper bonding wire offers high electrical and thermal conductivity and a lower rate of inter-metallic compound growth, providing superior reliability in high temperature environments compared to gold bonding wire. Copper offers lower bulk resistance (electrical), increased operating current and greater bond stability compared to gold, and has an improved lifetime at 180°C. Further, from a cost perspective given current gold pricing, copper bonding wire is about one-tenth (or less) the cost of gold bonding wire, depending on the wire diameter. The adoption of copper bonding wire, however, requires a process change in terms of tool sets. Inert gas supply is needed for ball formation to prevent oxidation of copper bonding wire.

The price of gold wire is just one example; rising material (and energy) pricing is also affecting the price of leadframes, laminate substrates, encapsulants, and other materials. As a consequence, device manufacturers, their outsource manufacturing partners, and material suppliers must dedicate resources to developing processes and materials for cost reduction.

Throughout the industry supply chain, companies struggle to pay for the innovation needed to advance materials technology. In addition to being affected by higher starting material costs, companies are squeezed from the top, where the end consumer demands lower cost electronic goods, which results in pressure to cheaper semiconductor devices. This leads to the second significant challenge related to material technology and development.

Material formulation and process development/integration require considerable R&D resources. Any new

## Regional Semiconductor Packaging Materials Markets



Region	2007E \$B	2008F \$B	% Change
China	1.98	2.39	21%
Europe	0.64	0.67	5%
Japan	3.11	3.25	5%
Korea	1.97	2.07	5%
Americas	0.58	0.60	3%
Taiwan	3.64	4.03	11%
Southeast Asia	5.00	5.43	9%
<b>Total Regions</b>	<b>16.92</b>	<b>18.44</b>	<b>9%</b>

Totals may not add due to rounding

continued from page 9

material introduction experiences a long adoption cycle between the time of its initial design and development to full production. Added challenges include the minute amount of material required in some processes; a consolidating customer base; and unique and customer-specific material requirements. So materials development drives a heavy R&D commitment, while the possibility of pursuing along a “blind alley” raises the risk, for a given supplier, that a Return-on-Investment (ROI) may not be realized.

The 2006 update to the International Technology Roadmap for Semiconductors (ITRS) notes that “increased device complexity requires higher cost packaging solutions,” though margins in the industry are inadequate to support innovation. With the surge in the types and sizes of packages, materials intensity in the back-end is growing, so solutions driving innovation are needed. Collaborative efforts, in various forms such as through consortia or company-to-company, allow companies to share risks and R&D costs so to keep pace in developing new materials.



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# Aspects on Advanced Thermal Management for Flip Chip on LTCC

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## Abstract

One of the major driving forces for the electronic industry is consumer handheld units, where more and more functions in a smaller volume and with longer battery time are requested. This leads to a higher energy- and interconnect density. One trend to manage the interconnect density is using Flip Chip (FC) technology which remarkably reduces the keep out area around the die compared to a wire bonded one. Two challenges related to this request that the industry is facing are thermal management and reliability. This paper will discuss some aspects of using FC technology on Low Temperature Cofired Ceramics (LTCC) for this kind of product and will focus on the heat dissipation problem of a FC mounted die. Test designs were developed and built to investigate SnAgCu (SAC) bumps on five different LTCC designs and the thermal influence of underfills. The LTCC design parameters were thermal vias and heat spreaders. In the experimental part the semiconductor junction temperature was measured over a diode in the semiconductor. Furthermore cross sectioning, X-ray imaging and infrared thermal imaging were used. The experiments were accompanied by FE-modeling using ANSYS workbench.

**Keywords:** Low Temperature Cofired Ceramics, Flipchip, Thermal Management, Reliability, FE-modeling

## Introduction

The LTCC technology is a multilayer ceramic technology, with vias as interconnects. The vias can be used as an electrical and / or thermal conductor. On the LTCC different interconnection technologies for the semiconductor assembly, such as wire- or FC-bonding can be applied. Due to the fact that semiconductors generate heat while operating, the thermal management must be considered. In a wire bonded solution the die is mounted with the backside on a heatsink. In the flip chip technology, where the backside faces up, the heat must be transferred through the solder bumps and the underfill down to the substrate. For FC applications in the LTCC module technology the FC backside can not be used as heatsink from space prospective [1].

In order to characterize a standard FC LTCC module a test structure was designed and fabricated. The test module contains a FC mounted thermal test die. The test die has an integrated heating resistor and a diode to monitor the junction temperature. For the tests, the die was underfilled using a commercial standard underfill. The underfill was optimized for reliability and not for thermal matter.

A daisy chain, which leads through the LTCC, the solder bumps and the die is also integrated in the test designs. The structure of the samples is shown in Figure 1.

## Results and Discussion

The investigation parameters are the thermal vias, the heatspreaders, the LTCC thickness, the underfill, the via offset, the via offset position, and the standoff height. Figure 2 defines some of the different param-

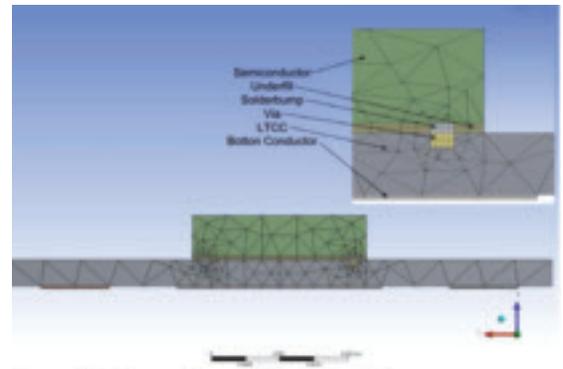


Figure 1: Overview of the test design.

eters. The via diameter in the test setup was 100 microns and in order to simulate a possible via misalignment during the fabrication process, the via offset was varied between 0 and 100 microns and the offset heights between 50 microns below the top layer and 50 microns above the bottom layer. One further parameter which was tested was the standoff height. The standoff height mainly depends on the Under Bump Metallization (UBM) diameter, the solder bump volume, the substrate planarity, the bump planarity, the wetting angle and the via diameter.

Increased standoff height has a positive influence on the temperature cycling behavior, but a negative on the thermal management, so there must be a tradeoff here [3, 4].

For the measurement each set of samples was soldered on to a brass plate which acts as a reservoir at

25°C and the heating resistor was powered with 1W. Then the voltage drop over the integrated diode was measured and the semiconductor junction temperature was calculated using Equation 1.

$$\begin{aligned}
 U_D &= \text{diode voltage [V]} \\
 T_M &= \text{measured die temperature [°C]} \\
 T_M &= (U_D - 0,70085) / -0,00208 \quad (1)
 \end{aligned}$$

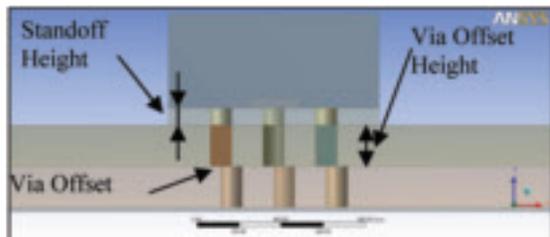


Figure 2: Overview of the different parameters for the experiment.

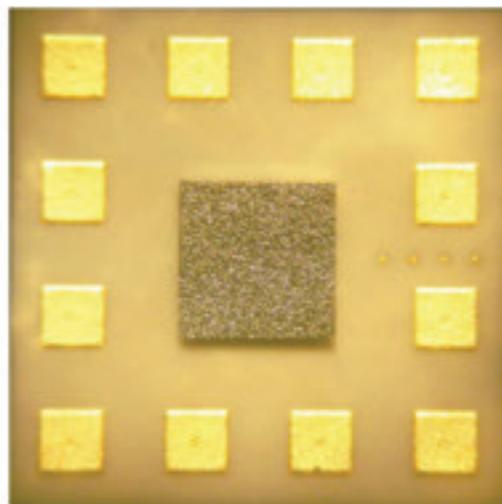


Figure 3: Sample of a thermal test die mounted with flip chip technology on a LTCC-substrate.

The nomenclature for the samples is XYZ.

Where:

- X ➤ Substrate thickness: A=400µm, B=800µm and C=1200µm
- Y ➤ Design option: 0,1,2,3 and 4. See Table 1 below.
- Z ➤ Underfill: U=underfill or N=no underfill

The test vehicle without underfill is shown in Figure 3 and Figure 4. Note that the four open vias to the right indicate the options of the designs which are shown in Table 1.

Design option	Additional thermal vias	Heat spreader structures
4	Yes	Yes
3	No	Yes
2	Yes	No
1	No	No
0	Only electrical routing in the first Layer ➔ No thermal vias or heat spreader	

Table 1: Design Options

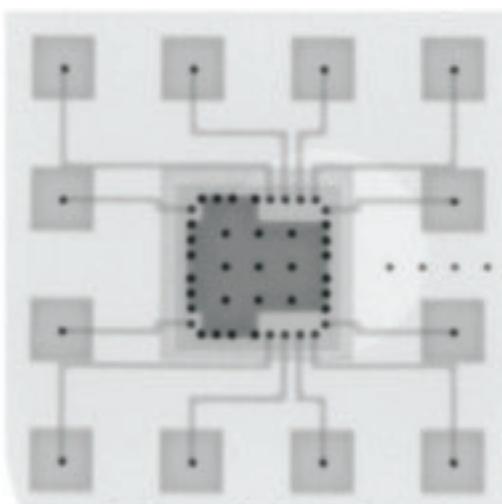


Figure 4: X-ray investigation of the thermal test FC die mounted on the LTCC. The 9 inner vias were optional as additional thermal vias (see Table 1).

The effect of using underfill or not is shown in Figure 5. There is a small but not significant decrease in the junction temperature. The used underfill was optimized for reliability and not for thermal matter and the thermal conductivity was only 0.3W/mK.

The LTCC substrate thickness was varied between 400 microns and 1.2 mm. The measurements of the semiconductor junction temperature versus the LTCC substrate thickness are shown in Figure 6. Increasing the LTCC substrate thickness from 400 microns to 800 microns results in a 5 K higher junction temperature.

The results for the five different thermal designs described in Table 1 show that the thermal vias have the major effect on the thermal management (see Figure 7). By adding heatspreaders and / or additional thermal vias (design 1..4) the effect on the thermal management is only minor and not significant.

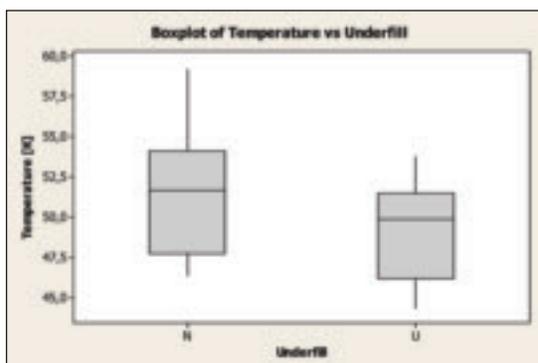


Figure 5: Semiconductor junction temperature rises above ambient for the underfilled case versus the not underfilled case.

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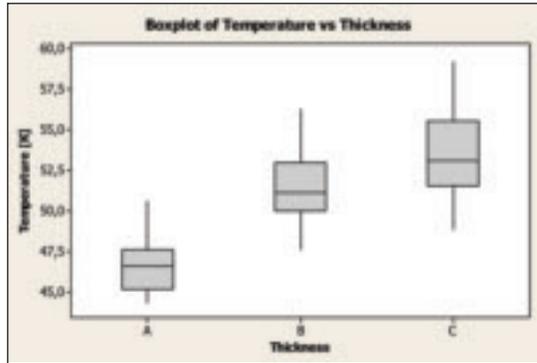


Figure 6: Semiconductor junction temperature rises above ambient for the three different LTCC - thicknesses.

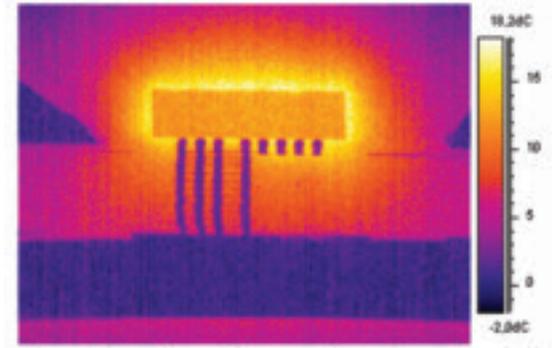


Figure 8: Infrared image of a FC mounted die on LTCC substrate with thermal vias and heatspreader.

Figure 8 shows an infrared image of a cross sectioned test sample. The picture shows the result of a subtraction of the image at powered state minus the one in a non powered state. The temperature distribution in the picture clearly points out the distinct influence of thermal vias and heatspreaders.

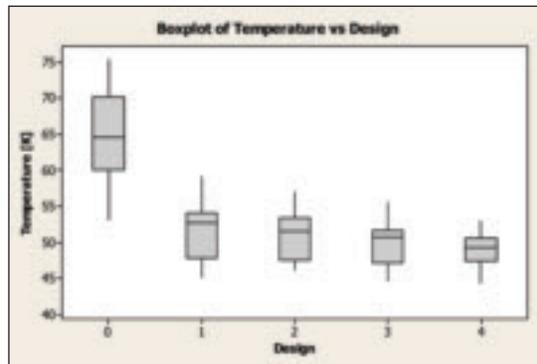


Figure 7: Semiconductor junction temperature rises above ambient for the five different thermal designs.

For each combination of parameters a set of 5 samples was measured and a supporting FE-Modeling was done [5]. Figure 9 shows the results for the via offset and offset height.

The measurement and simulation shows a good accordance and demonstrates that a via offset smaller than 60 microns gives only a slight temperature increase, regardless of the via offset height. At 100 microns offset the influence of the offset height is visible. The influence gets stronger while the offset gets closer to the heat source.

The influence of standoff height is shown in Figure 10. The semiconductor junction temperature is directly proportional to the standoff height, but the influence is rather small.

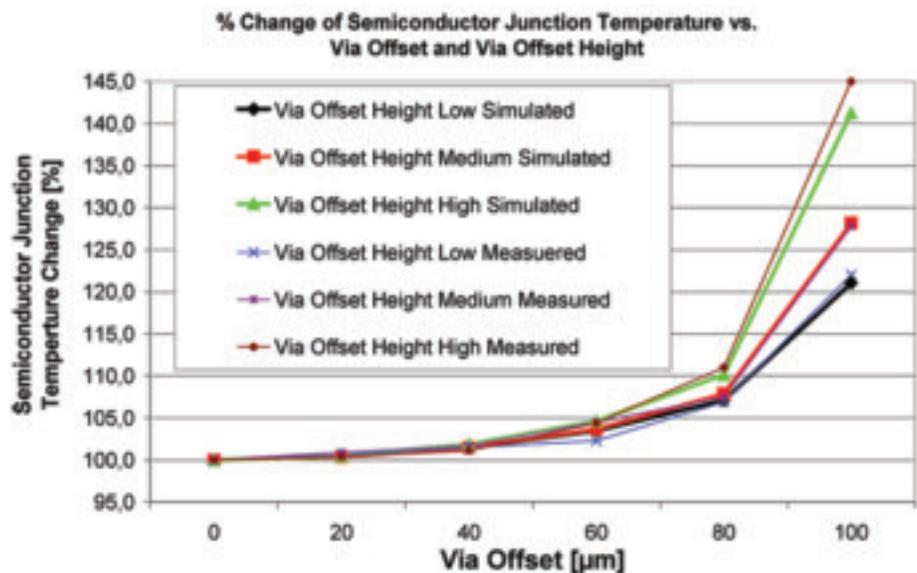


Figure 9: Measured and simulated % change of the semiconductor junction temperature vs. via offset and offset height.

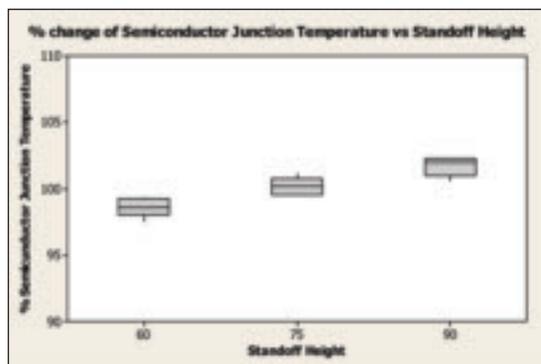


Figure 10: Measured % Change of the semiconductor junction temperature vs. stand off height.

### Conclusions

To minimize the semiconductor junction temperature in the package, the combination of material and thermal design must be considered. The main reduction of the temperature is related to the usage of thermal vias. A via offset smaller than 60 microns with a 100 microns vias diameter gives only a minor increase in the semiconductor junction temperature. Reducing the LTCC substrate thickness will decrease the junction temperature further. This paper showed that FC on LTCC is a promising key technology for power amplifier modules e.g., PaiD (Power amplifier with integrated Duplexer).

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# A Local, Reactive Heat Source for Room Temperature Soldering of High Power Devices to Substrates

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With increasing power density and higher heat dissipation requirements in power electronic components, minimizing the thermal resistance at the component-to-heat sink interface is critical to more effectively cool the component for long-term reliability [1,2,3]. In response to these high demands on the thermal interface, a new generation of low thermal resistance interconnect materials based on reactive multilayer bonding (NanoBond®) has been developed.

This novel process uses reactive multilayer foil (NanoFoil®) to solder components in less than a second, in air, at room temperature, with minimal thermal exposure to the components. Reactive multilayer foils are a class of nano-engineered materials fabricated by vapor depositing hundreds of nanoscale layers that alternate between elements with large negative heats of

mixing, such as nickel (Ni) and aluminum (Al) (Figure 1). Heat is generated by initiating a self-propagating exothermic reaction in the foil via a small energy impulse [4]. The thermal energy produced by the reaction rapidly melts adjacent solder layers, bonding the components [5]. These solder bonds have high thermal conductivities as well as low thermal contact resistances associated with the metallic wetting of the components by the solder.

In this article, we describe the use of reactive multilayer foils to solder-bond two different high power devices to heat spreaders/sinks, including the bonding of high brightness LEDs to metal core printed circuit boards (MCPCBs), as well as the bonding of bare-die GPUs to heat sinks. We discuss the thermal performance and reliability test results for reactive multilayer

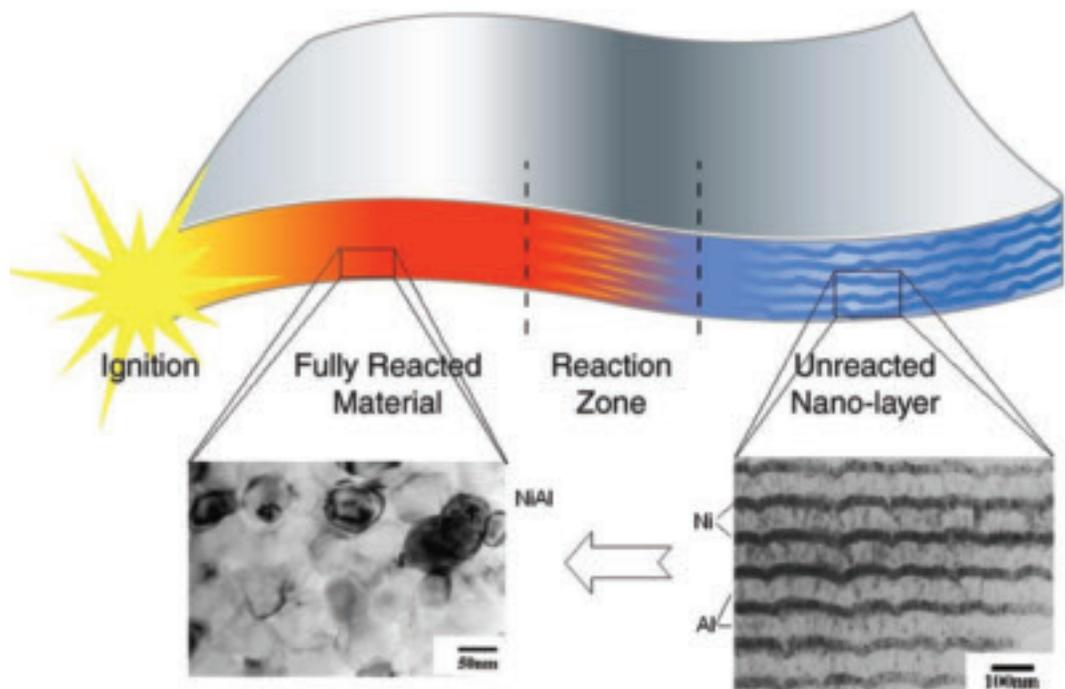


Figure 1. Schematic of reacting multilayer foil (NanoFoil®), ignited on the left, wave propagating to the right, with microstructures before and after reaction.

bonds and present comparisons of thermal performance between these bonds and other current market solutions. The test results show that the introduction of a reactive multilayer bond as a thermally conductive interconnect material between the high power device and the heat sink demonstrates significant performance advantages over other current commercially available TIM (Thermal Interface Material) solutions.

### Bonding of High Brightness LEDs to MCPCB Boards

Previous studies have shown that the temperature at the junction of an LED determines the light output, spectral shift, and degradation of light output over time [3,6,7]. In this study we solder bonded OSRAM Dragon-series LED packages to MCPCBs using reactive multilayer foil, demonstrated the reliability and quality of the bond in this application, and compared its thermal performance with that of commercial thermal adhesives. The joining configuration used for the reactive multilayer bond is shown in Figure 2.

The strength and thermal performance of the reactive multilayer bond was optimized by varying the multilayered foil thickness and bond process parameters such as bonding pressure. The resulting optimized bonds exhibit average measured thermal conductivities of 30W/Km and shear strengths of 35 MPa (5130 PSI) with average less than 5% void content (Figure 3). There is no significant degradation observed in the thermal performance and structural performance after a series of reliability tests. The reliability test results are detailed in Table 1.

Comparative thermal resistance tests were carried out between reactively bonded LED packages and the epoxy thermal interfaces currently utilized. The tests were conducted on 1.6W Golden Dragon LEDs attached to MCPCBs, and the thermal tests using thermal transient testing [8]. Preliminary testing shows the reactive multilayer bonds dramatically outperform thermal epoxy with one third of thermal resistance from junction to MCPCB. With further optimization the performance gap between the reactive bonds and thermal epoxy may be even larger. This improvement in thermal resistance will result in a lower operating temperature for the LED die than the current thermal

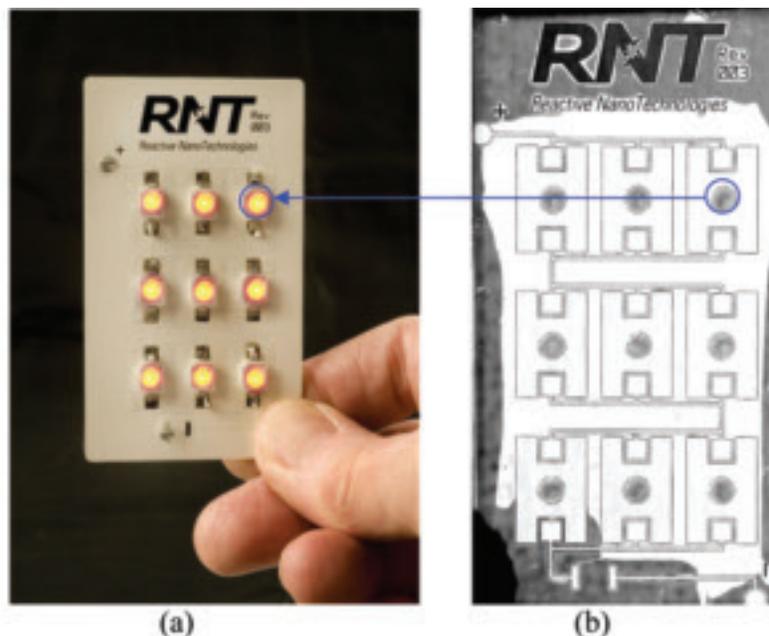


Figure 3: (a) LED packages bonded with reactive multilayer foil to Sn-plated MCPCB. (b) Acoustic microscopy (C-scan) image of an LED package reactively bonded to a MCPCB. The areas exhibiting dark contrast (an example of which is circled) represent bonds between the board and the metal slug at the base of the LED package.

adhesive solution, potentially increasing the lifetime of the LED devices.

### Bonding of Silicon Dies to Copper Heat Sinks

The joining configuration for the die to heat sink reactive bonding method is shown in Figure 4. Indium solder is used because of its high thermal conductivity and its ability to accommodate the thermal expansion mismatch between the silicon die and copper heat sink without degrading or applying significant stress to the components [9,10].

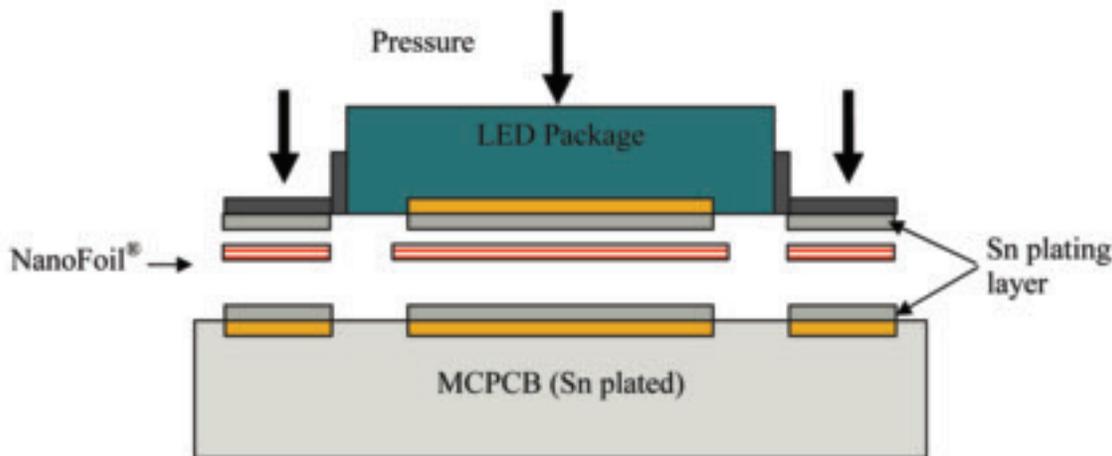


Figure 2: Diagram illustrating the LED reactive multilayer bond (NanoBond) process.

continued on page 18

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Table 1. Reactively Bonded LED Package Reliability Data

Test	Conditions	Standard	Result (Bond Quality)
Thermal Cycling	-40°C to +125°C, dwell = 15 min, 1000 cycles	JESD22-A104C	Passed
High Temp/High Humidity	TA = 60°C, r.H. = 90%, IF = 400mA	JESD22-A108	Passed
Mechanical Shock	500g, >4 ms	IEC 60068-2-27	Passed
Random Vibration	Sin 20 –1kHz >20g, 3 axes/1.5h each/500g >4ms	IEC 60068-2-6	Passed
High Temp Storage	TA = 125°C, 1000 hours	JESD22-A103C	Passed

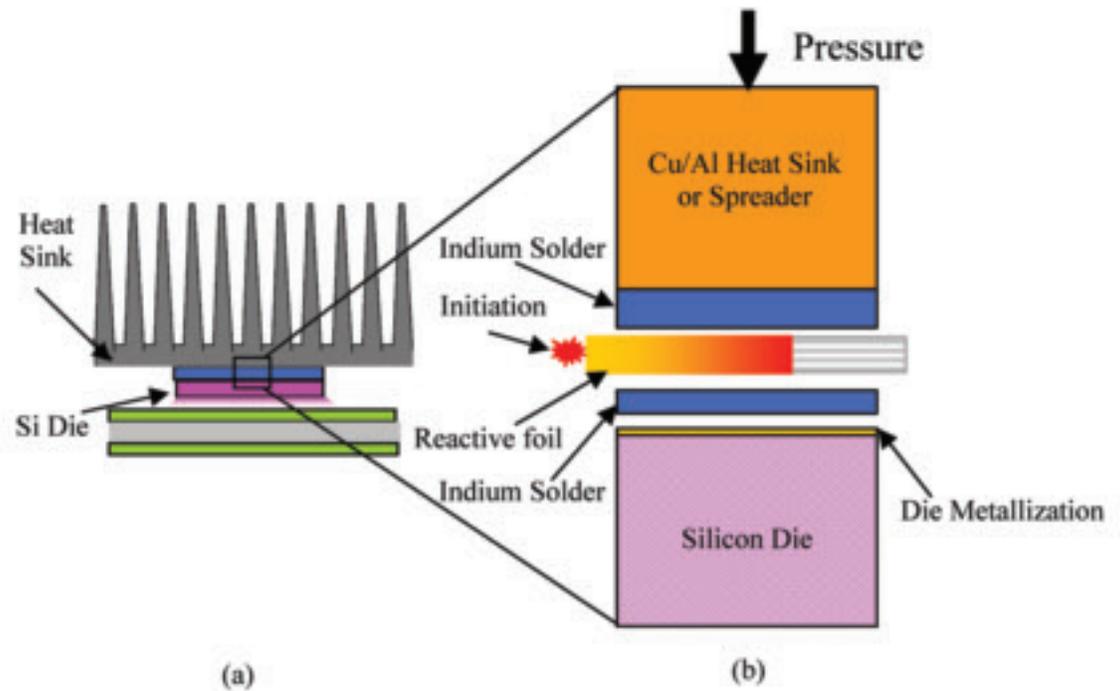


Figure 4. Reactive metallic joining of components to silicon dies for TIM applications. (a) Typical silicon chip and heat sink package. (b) Joining configuration used.

The thermal performance of the reactive multilayer bonds was measured using a laser flash technique. In addition a series of reliability tests were performed on the bonded samples including temperature cycling, thermal shock, mechanical shock, vibration and temperature-humidity bias tests. The bonds have average measured thermal resistances of 0.04-0.05 K cm<sup>2</sup>/W with a standard deviation of less than 0.003 K cm<sup>2</sup>/W. The results of reliability tests are summarized in Table 2, and show that there is no significant degradation observed in the thermal performance after reliability testing.

To obtain a direct comparison of the thermal performance of reactively bonded GPU interfaces with current commercially available TIM solutions, benchmark testing was performed using an operational video card as a test vehicle. The performance of a reactive bond was tested against two high-end commercial greases, one phase change material (PCM) and one low melting alloy (LMA). The test results are listed in Table 3. The thermal resistance of the reactive bond is roughly one fifth that of organic grease A, a quarter that of grease B, and a third that of the phase change material and low melting alloy.

Table 2. Silicon Die - Copper Heat Sink Bond Reliability Test Summary

Tests		Test Conditions	Thermal Resistance before Test* (K-cm <sup>2</sup> /W)	Thermal Resistance after Test* (K-cm <sup>2</sup> /W)
Temp Cycles	208µm BLT	0-100°C, 3000 cycles (JESD22-A104C)	0.049	0.047
	154µm BLT		0.043	0.046
	125µm BLT		0.043	0.047
Thermal Shock		-50°C – 100°C, 30s each status, 100 shocks	0.042	0.041
Mechanical Shock		50g, 5ms, half-sine, in six axes (IEC 60068-2-27)	0.041	0.041
Vibration		Random, 5 Hz at 0.01 g <sup>2</sup> /Hz, 20 Hz at 0.02 g <sup>2</sup> /Hz, and 500 Hz at 0.02 g <sup>2</sup> /Hz, 10 minutes per axis (IEC 60068-2-6)	0.038	0.038
High Temp/ High Humidity		85°C / 85%, 1000 hrs (JESD22-A108)	0.036	0.034

\* Repeatability and Reproducibility of laser flash unit +/-5%

## Conclusions

Reactive multilayer bonding is demonstrated to be a robust thermally conductive interconnect solution to attach high power devices to the heat sinks or MCPCBs. The thermal performance of a reactively bonded commercial LED package to MCPCB is 3X better than that of the current epoxy solution and the thermal performance of a reactively bonded GPU to heat sink measured by benchmark tests is up to 3X - 5X better than those of other market available TIM solutions. The bonds made using this local heating technology also passed a series of industrial standard reliability tests.

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Table 3. Benchmark Test Thermal Performance Summary

TIM	Maximum Junction Temp.	Avg. Inlet Temp.	ΔT (Max. junction-inlet)	Interface Resistance
	°C	°C	°C	°C/W
Reactively bonded (NanoBond)	92.1	28.1	64.1	0.015
Organic Grease A	95.2	28.7	66.5	0.072
Organic Grease B	95.0	28.8	66.2	0.066
PCM (Indium-based)	93.5	28.4	65.1	0.041
LMA (Indium-based)	92.8	27.7	65.1	0.041

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# The Role of Interfacial Compound Formation on Package Reliability

Jonathan H. Harris and Erich Rubel, CMC Interconnect Technologies

Since all types of electronic packages involve the bonding of heterogeneous materials, interfaces between different material types frequently have a significant impact on package performance characteristics. Interfacial requirements in packaging applications can take on a number of different aspects. These include adhesion strength of the interface, mechanical stability when stressed (for example, temperature cycling or mechanical shock), transmission of heat through the interfacial layer and the chemical stability of the interface during processing or in the work environment. The focus of this paper will be to discuss the impact of specific chemical compounds that frequently form at metallization interfaces in packaging applications on the reliability of those interfaces with respect to the type of interfacial requirements listed above.

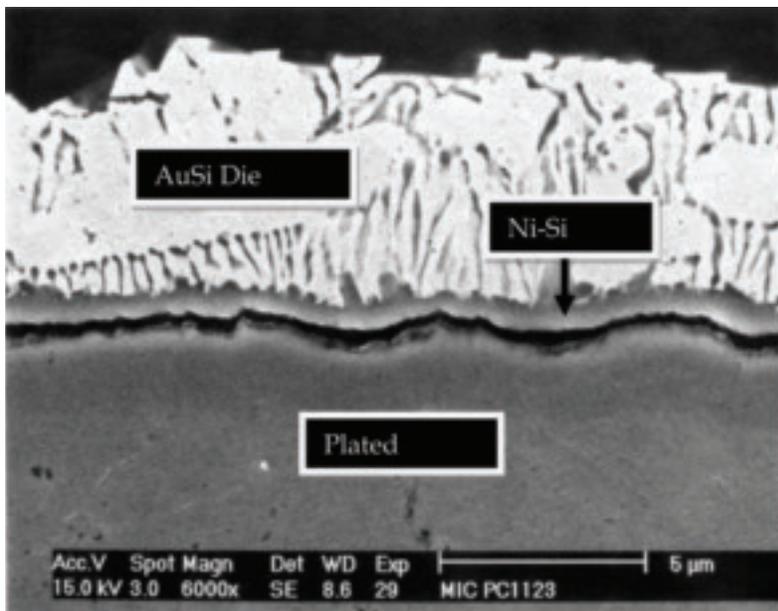


Figure 1: Single Mode Failure between Die Attach and Plated Layers

## Interfacial Failure Modes

Figure 1 shows interfacial failure between a AuSi die attach layer and the underlying Ni plating.

In this case, a single mode of failure is observed: delamination along the interface between the AuSi layer and the Ni plated layer. In general, this type of failure can have different origins: poor adhesion of the two components due to contamination or inappropriate material choices; or the presence of a brittle, continuous phase at the interface between the two metal layers which fractures when stress is applied to the interface. In fact, in Figure 1 the interfacial failure is caused by the presence of a continuous nickel silicide layer between the Ni plated layer and AuSi. This nickel silicide ( $\text{NiSi}_2$ ), which is an example of an intermetallic compound (IMC), is brittle and fractured when the interface was exposed to a shear force. Clearly this type of single mode failure directly through the interfacial region is a potential reliability concern, regardless of the force required to instigate this failure. This article will focus on the role of IMC formation in precisely this type of stress-induced interfacial failure.

## Intermetallic Compounds

Intermetallic compounds (IMC) are ordered alloy phases made up of two or more metal components with a narrow composition range (line compounds in a phase diagram). Each distinct metallic atom in the IMC structure occupies a specific site on the crystal lattice.

The copper-silicon phase diagram is shown in Figure 2<sup>1</sup>. This system exhibits a number of different IMC composition including:  $\text{Cu}_{33}\text{Si}_7$ ,  $\text{Cu}_{16}\text{Si}_4$ ,  $\text{Cu}_9\text{Si}_2$ , and  $\text{Cu}_{19}\text{Si}_6$ .

Because IMCs of relevance to electronic packaging metallization systems often form in-situ during metal interface formation, and often under non-equilibrium conditions, it is very difficult to fabricate bulk IMC samples with the same crystalline composition and grain structure as interfacial phases. For this reason, the bulk properties of many interfacial IMC materials have not been well characterized.

One study performed by Fields and Low<sup>ii</sup> at NIST Metallurgical Division attempted to reproduce compositions and microstructures of CuSn and NiSn IMCs found at metallization interfaces. A summary of the data from their study is shown in Table 1.

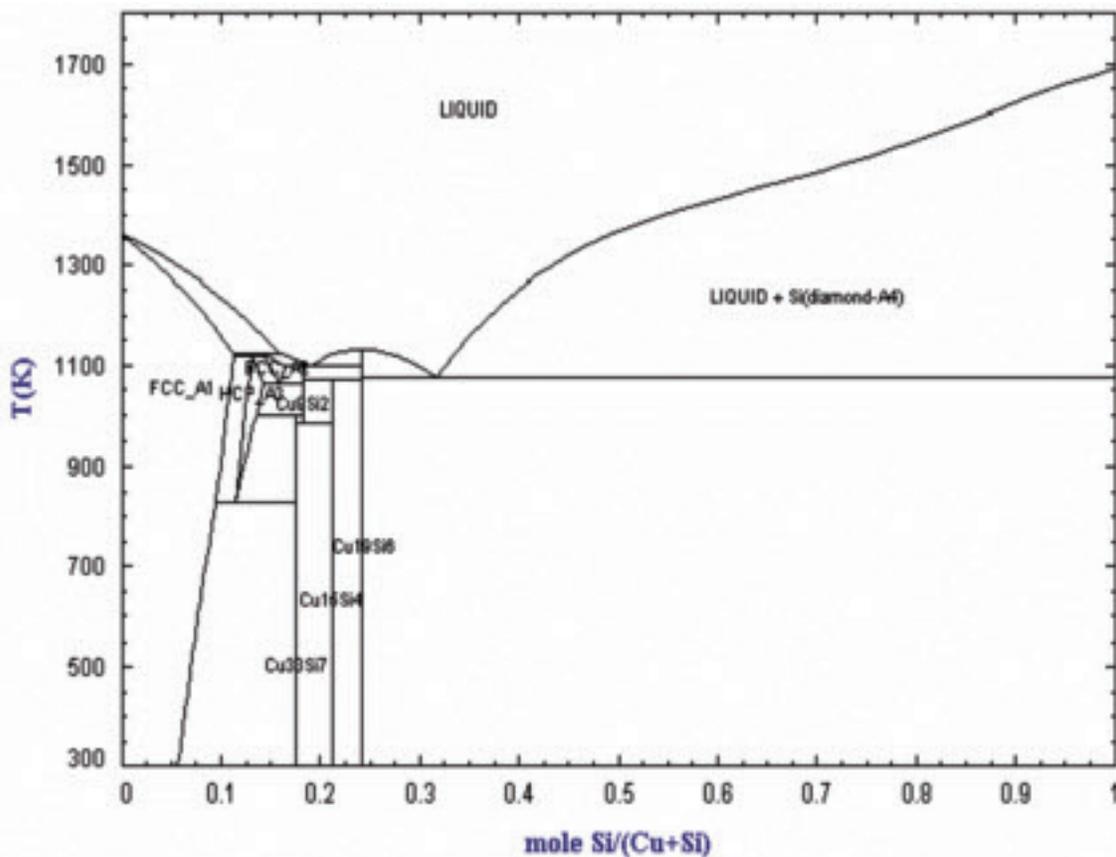


Figure 2: The Copper Silicon Phase Diagram

There are a number of important material trends that are illustrated by the data in Table 1. The first key trend is that an IMC formed from two ductile elements can be very brittle. In this case, the parent elements Cu and Sn are ductile, but when they react to form  $Cu_6Sn_5$  and  $Cu_3Sn$ , the resultant IMC is brittle. Another trend that is associated with IMC formation is severe degradation of both thermal and electrical conductivity. In this case, Cu has a thermal conductivity of 385 W/m-K which falls by a factor of more than 5 when  $Cu_3Sn$  is formed. This is very close to the thermal conductivity of pure Sn (67 W/m-K). The same type of drop is seen in electrical conductivity.

It is very clear from this brief discussion why IMC formation can be such a serious issue for electronic packaging metallization interfaces. Mechanical integrity, thermal conductivity and electrical conductivity are all critical parameters for effective package performance. If a continuous IMC layer forms as part of the metallization, particularly if the IMC layer is thick, very significant degradation in device performance and reliability can be observed. For packaging applications, this could be a die attach metallization or interconnection of a lead, wirebond pad or heat spreader. Specific examples of this type of degradation in electronic packaging applications will be discussed later in this paper.

Property	$Cu_6Sn_5$	$Cu_3Sn$	$Ni_3Sn_4$	Cu
Vickers Hardness (Kg/mm <sup>2</sup> )	378 (+/- 55)	343 (+/- 47)	365 (+/-7)	50
Mechanical Character	Brittle	Brittle	Brittle	Ductile
Poisson Ratio	0.309	0.299	0.330	.34
Thermal Expansion (ppm/c)	16.3	19.0	13.7	16
Thermal Conductivity (W/m-K)	34.1	70.4	19.6	385
Resistivity (micro-ohm-cm)	17.5	8.93	28.5	1.7
Density (g/cc)	8.3	8.9	8.65	8.9

Table 1: Key Properties of Various CuSn and NiSn IMCs (from Reference X)

continued from page 21

Layer	Typical Layer Constituents	Possible IMC Compositions Forming Between Layers
<b>Bonding</b>	Ti, W, Cr	
<b>Diffusion Barrier, Solder Wetting Layer</b>	Ni, Pd, Pt, Cu	Ti <sub>2</sub> Ni, TiNi <sub>3</sub> , Ti <sub>2</sub> Pd, Ti <sub>2</sub> Pd <sub>3</sub> , TiPd <sub>5</sub> , Ti <sub>2</sub> Cu, Ti <sub>2</sub> Cu <sub>4</sub>
<b>Solder, Wirebond or Die Attach</b>	Au, AuSn, AuSi, Ag-Sn-Cu	Ni <sub>3</sub> Sn, Ni <sub>3</sub> Sn <sub>2</sub> , Ni <sub>3</sub> Sn <sub>4</sub> , NiSi, NiSi <sub>2</sub> , Pd <sub>5</sub> Si, Pd <sub>9</sub> Si <sub>2</sub> , Pd <sub>3</sub> Si, Pd <sub>2</sub> Si, PdSi, Pd <sub>3</sub> Sn, Pd <sub>2</sub> Sn, PdSn, PdSn <sub>2</sub> , PdSn <sub>3</sub> , PdSn <sub>4</sub> , Pt <sub>6</sub> Si <sub>5</sub> , PtSi, Pt <sub>3</sub> Sn, PtSn, Pt <sub>2</sub> Sn <sub>3</sub> , PtSn <sub>2</sub> , PtSn <sub>4</sub>

Table 2: IMC Formation at Electronic Packaging Metallization Interfaces

### IMC Formation at Electronic Packaging Metallization Interfaces

Why is IMC formation a significant issue in electronic packaging applications?

Typically thin film metallization systems are comprised of three distinct functional layers. The first layer is designed to bond with the substrate; the second layer has two functions. It prevents diffusion of the bonding layer material into the top solder surface, and it also acts as a solder wetting surface. The top layer is hard or soft solder or Au for wirebond or soldering applications.

Table 2 lists typical elements or compounds that are found in these metallization layers. The table also illustrates, for different combinations of these elements or compounds, the numerous intermetallic compounds that have the potential of forming at each interface.

Note that we have only listed the binary IMC phases that can form in Table 2. There are also numerous ternary IMCs that can (and do) form in packaging applications. It is clear from this table that minimizing the negative impact of IMC formation on metal adhesion, electrical performance and thermal conductivity is a key priority in defining packaging metallization systems and processing.

### Examples of IMC Formation in Packaging Applications

#### AuSi Die Attach

One very informative example of how IMC formation can impact reliability and how IMC formation can be minimized using material know-how is AuSi die attach. AuSi is frequently used as a high thermal performance die attach material for high power microwave and RF silicon-based devices. For example, silicon LDMOS transistors that are used in cellular infrastructure applications use this die attach material. The advantage of AuSi compared to other die attach options is a thermal conductivity of 190 W/m-K. This is much higher than AuSn at 57 W/m-K. The disadvantage of AuSi is a very high processing temperature. The eutectic temperature of the Au<sub>80</sub>Si<sub>20</sub> eutectic is 363C and die bonding is typically done at temperatures exceeding

400C.

The AuSi eutectic die attach bond can be formed “insitu” when a gold coated silicon device is bonded to a gold plated electronic package. The package construction in this case consists of a gold plated layer with a plated nickel under layer. The nickel layer is necessary to provide a wetting surface for the AuSi solder.

Figure 1 documents the results of a die shear test performed on a silicon die with AuSi die attach on a plated Ni surface. The figure documents the formation of a continuous, brittle NiSi<sub>2</sub> intermetallic compound phase which forms between the AuSi die attach layer and the plated Ni layer. When stress is applied to this interface, brittle fracture of the IMC results in clean delamination of the silicon die from the package (single mode failure).

This situation is changed dramatically when the plated nickel layer is doped with greater than 5% cobalt. Because the kinetics of Co-silicide formation is slower than Ni-silicide formation, this doping frustrates the formation of a thick, continuous layer of silicide (a thin NiSi<sub>2</sub> layer, less than 0.3 microns, is sometimes present but is too thin to lead to failure). The NiCo layer also acts as a barrier to Ni diffusion to the interface. Figure 3 shows a cross-section of a silicon die bonded with AuSi but with a NiCo plated layer. Note that the NiSi<sub>2</sub> is now isolated into discontinuous “blocks”. When die shear is performed on NiCo plated samples, a mixed mode failure is seen with areas of failure in the silicon die and areas of failure in the AuSi layer.

This example is interesting, because it illustrates a situation where the morphology of the IMC layer is altered, not the IMC chemistry, yet a dramatic improvement in metallization reliability is observed.

#### AuSn Die Attach

AuSn is commonly used as a die attach material for high thermal dissipation applications. For example, AuSn is exclusively used to bond laser diode submounts into telecommunications packages for fiber optic applications<sup>iii</sup>. AuSn is also utilized as a seal ring solder and is used to make solder interconnection in applications where a solder hierarchy or fluxless soldering is required. Since AuSn is processed at 320C,

joints formed with AuSn will not be disturbed by subsequent processing at lead-free solder temperatures (260C).

From a metallurgical perspective, AuSn is very different than the AuSi eutectic discussed in the previous example. Whereas the AuSi eutectic solidifies into a mixture of pure Au and pure Si, AuSn eutectic liquid solidifies into a mixture of two intermetallic compounds: Au<sub>5</sub>Sn and AuSn.

The following example illustrates reliability issues that can result when AuSn is bonded to a plated Ni layer. A Ni under layer is typically utilized for some die attach applications and for most lead attach and seal ring applications. Figure 4 shows the interface between the AuSn solder and plated Ni after temperature shock. Note in this figure that a single mode interfacial failure is observed.

The EDS spectrum in Figure 5 identifies the phase that is observed on both sides of the failure surface in Figure 4 as a Au-Ni-Sn ternary IMC.

The most likely composition of this ternary IMC is (Au<sub>0.5</sub>Ni<sub>0.5</sub>)Sn<sub>4</sub><sup>iv</sup>.

This example illustrates an important concept in understanding the reliability impact of IMCs at metal-lization interfaces: ternary IMC compounds, where one species substitutes on the lattice site of another species, generally have even worse mechanical, thermal and electrical properties when compared to binary IMC (with no substitution).

There is a simple reason for this degradation of properties in the ternary compound. When one species substitutes on the lattice site of a different atom, the difference in atomic radii of the two materials leads to a localized stress field around the substituted atom. In the case above, Au has an atomic radius of 2.88Å while Ni is 1.49Å. The localized stress due to the substitution of Ni for Au as Ni diffuses into the AuSn solder can be estimated by the simple approximation:

$$\text{Lattice Strain} = C(\text{crystal structure})(r_{\text{solvent}} - r_{\text{solute}})/r_{\text{solvent}}^2$$

C is a constant that is dependent on the crystal structure of the IMC alloy.

This lattice strain increases the brittleness of the material and also scatters electrons which degrade both thermal and electrical conductivity.

Thus there are two key messages in terms of minimizing the impact of IMC at interfaces: (1) minimized the thickness and continuity of the IMC phase formed along the interface; and (2) try to limit the formation of any ternary IMC compounds during material processing.

### Sn-Ag-Cu Solder

The final example discussed in this article is the case of a Sn<sub>96.5</sub>Ag<sub>3</sub>Cu<sub>0.5</sub> solder ball bonded onto a Au plated pad with a nickel plated underlayer. After ball shear, brittle failure is observed as shown in Figure 6.

Figure 7 shows EDS spectra from the top of the pad shown in Figure 6, and Figure 8 shows EDS spectra from the complementary failed surface of the solder ball.

Note that Figure 7 documents the presence of a NiSn IMC phase on the top of the pad after ball shear, and Figure 8 shows the presence of a ternary Ni-Cu-Sn

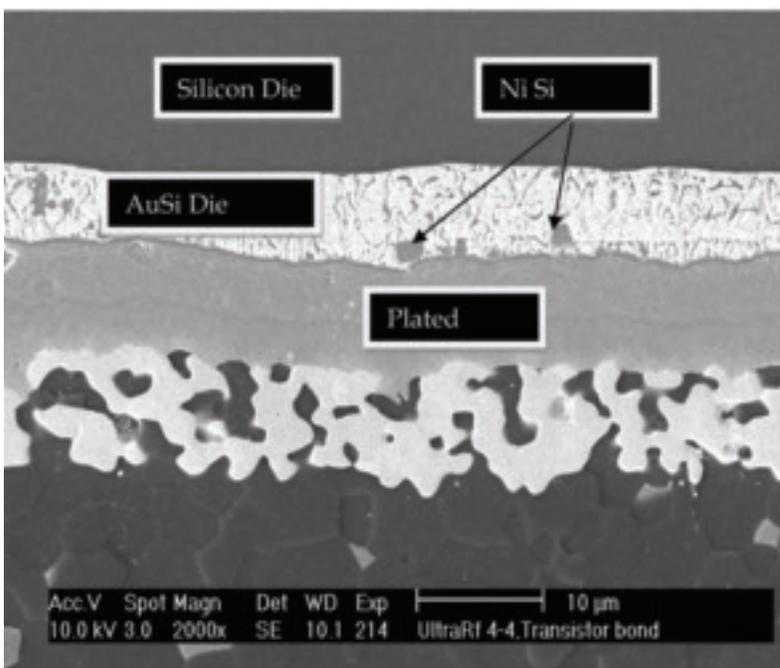


Figure 3: Doping Ni with Co Frustrates IMC Formation during AuSi Die Attach

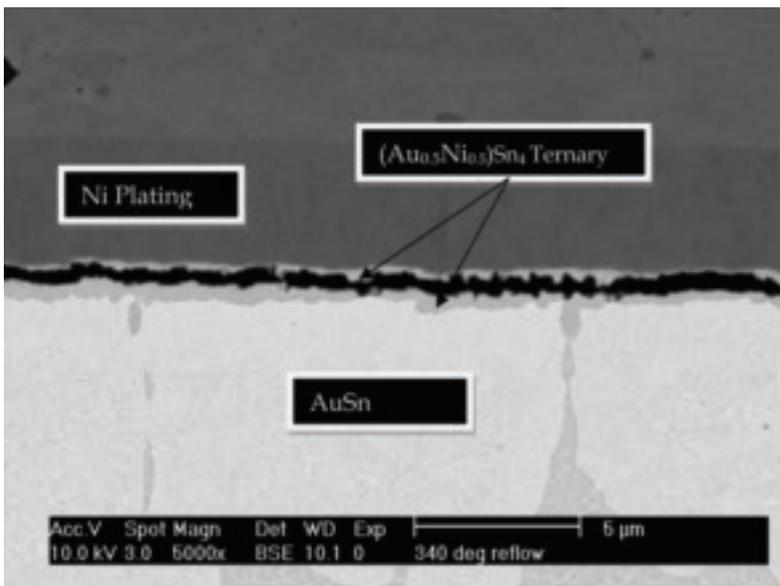


Figure 4: Failure at AuNiSn IMC when AuSn is soldered to Ni

IMC on the back of the detached ball. This indicates that the failure in this case occurred at the interface between two different IMC layers that formed when the Ni plated layer reacted with the SAC solder. These two distinct IMC layers are shown in cross-section in Figures 9 and 10.

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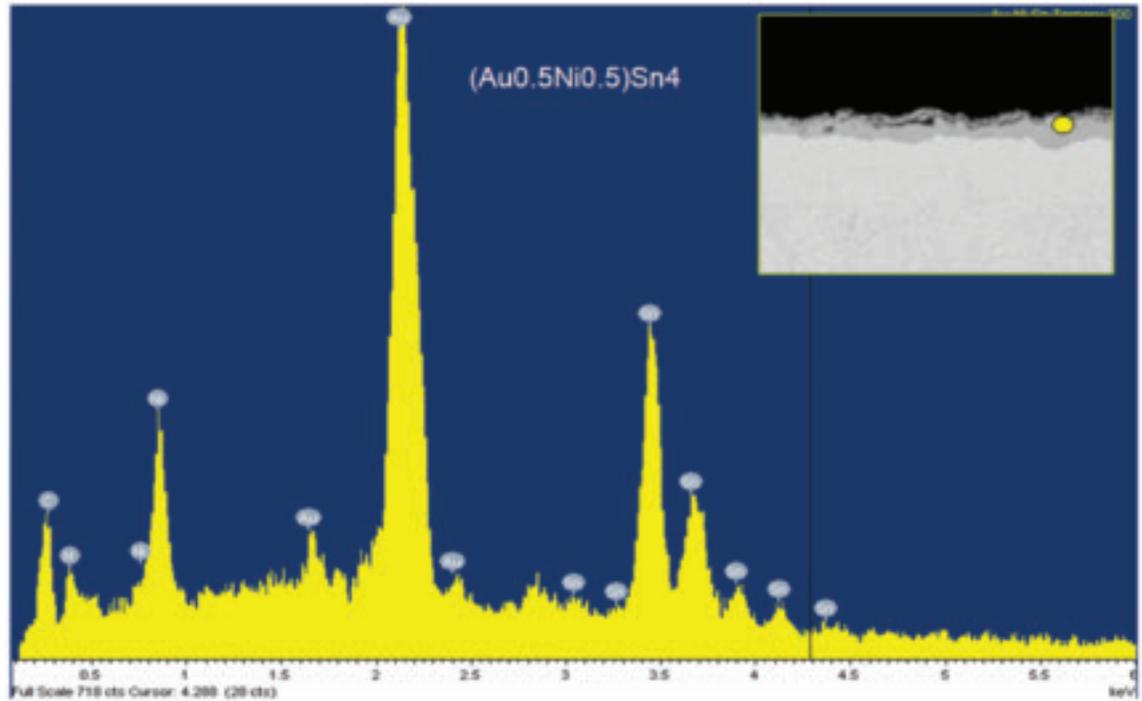


Figure 5: EDS Spectra of the Failure Interface when AuSn is soldered to Ni.

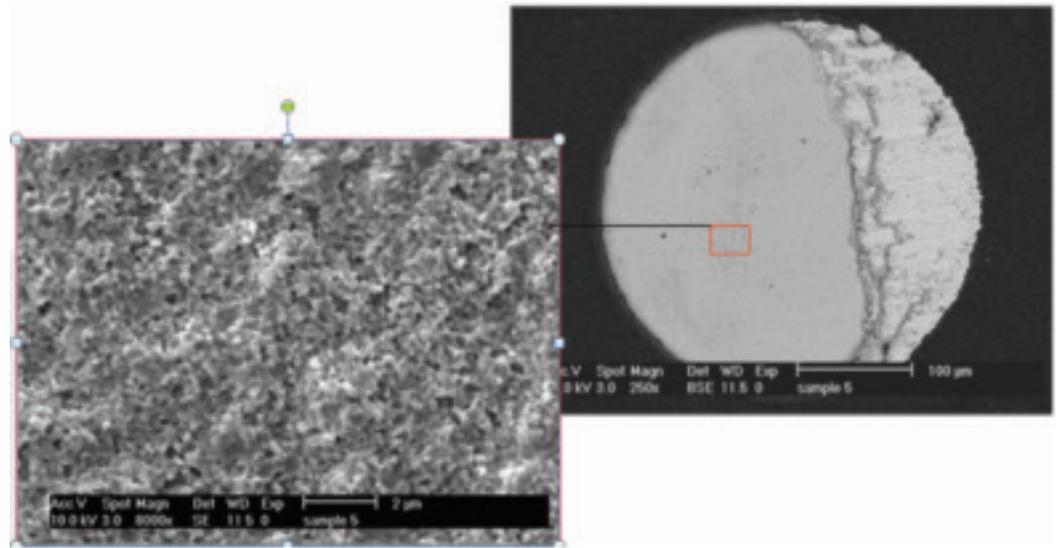


Figure 6: Top View of Pad Showing Ball Shear Failure

### Discussion

The failure analysis examples shown above illustrate a number of key concepts concerning IMC formation at metallization interfaces in electronic packaging applications:

- It is extremely difficult or impossible to eliminate IMC formation in electronic packaging applications. The groups of elements that are necessary to form effective interfaces in packaging applications (adhesion layers, bonding layers, solders) also

form numerous IMC when they interact with each other during bonding.

- Morphology of the IMC layer is critical. If the layer is continuous or excessively thick, brittle fracture can occur within the layer leading to delamination of the metallization. If the continuous layer can be interrupted, as was the case for Co doped Ni plating for AuSi die attach, then the reliability of the interface can be greatly improved.

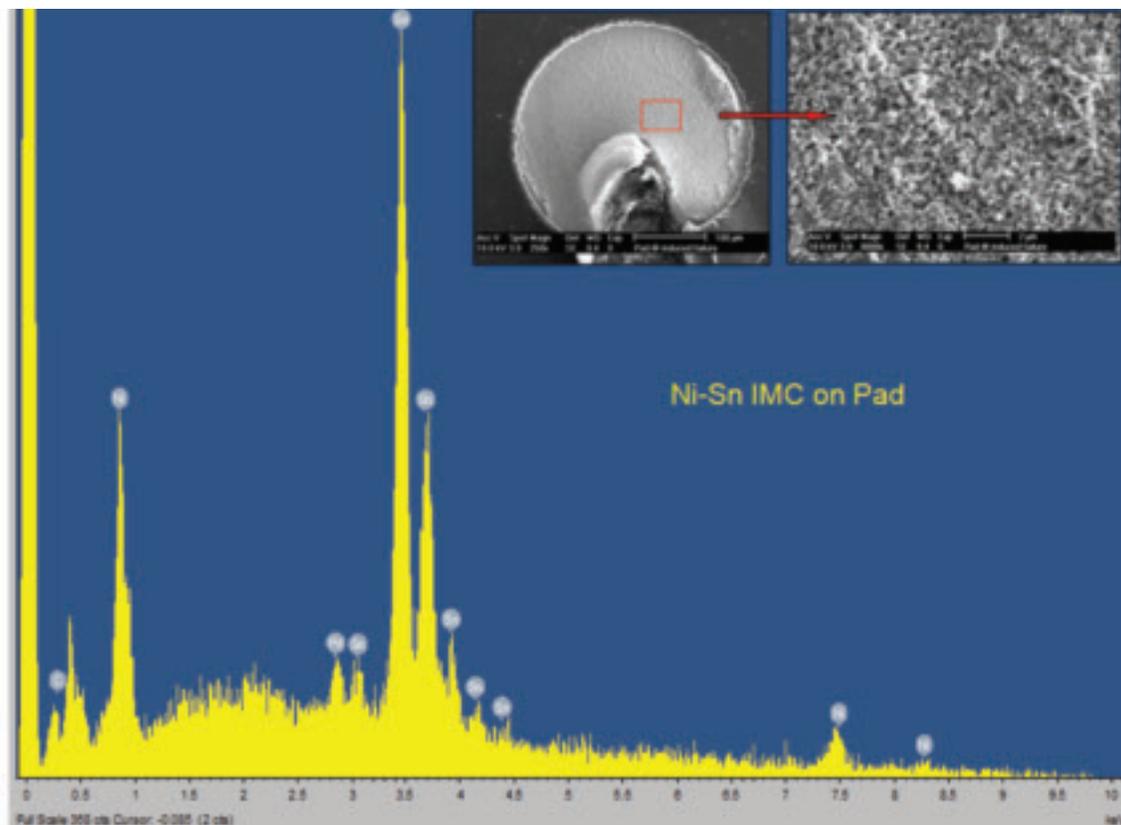


Figure 7: EDS Spectra from Top of Pad after Ball Shear

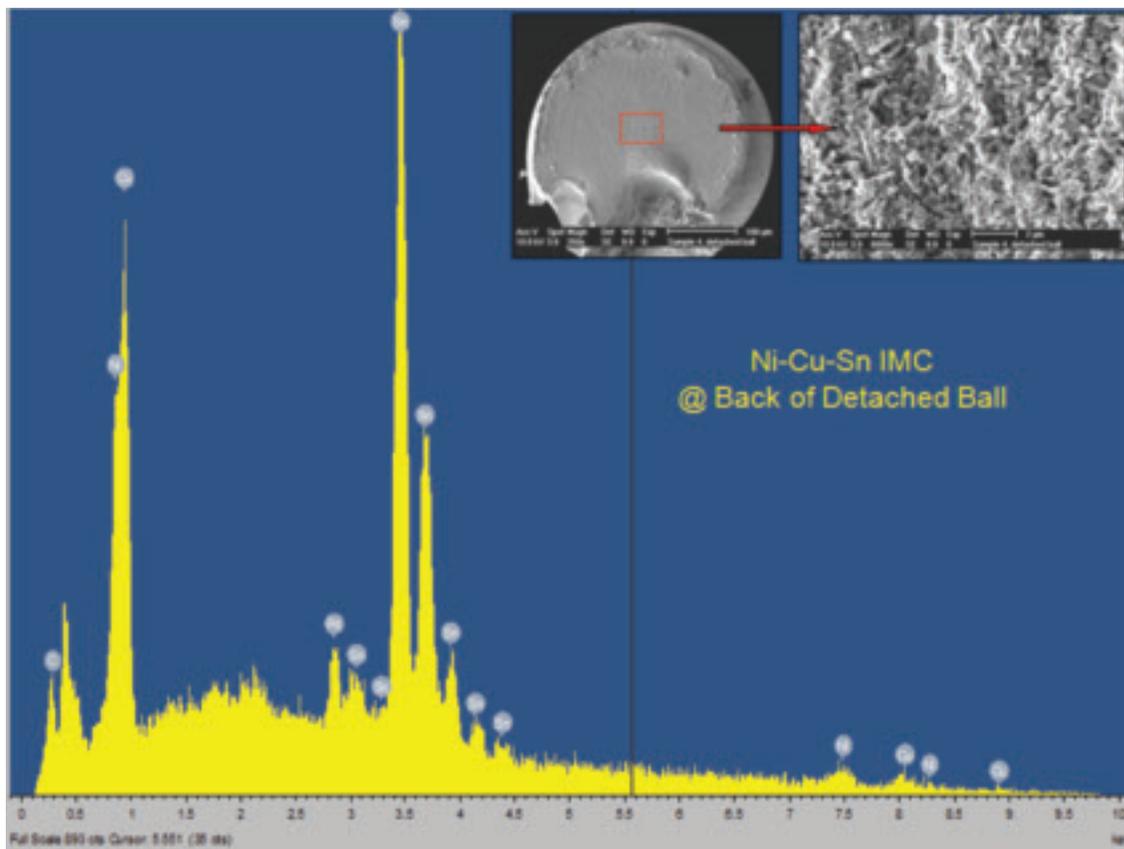


Figure 8: EDS Spectra from the Bottom of the Ball after Ball Shear

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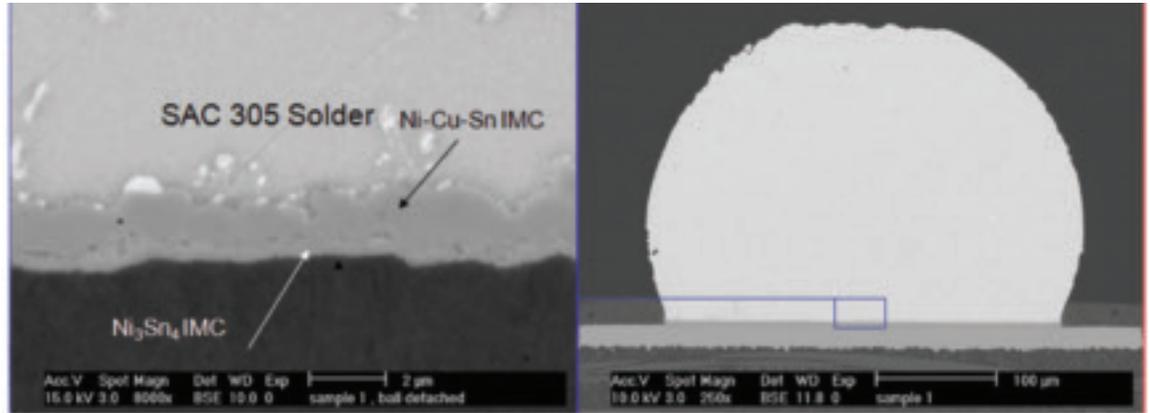


Figure 9: IMC Formed when a SAC Solder Ball is bonded to a Ni plated layer

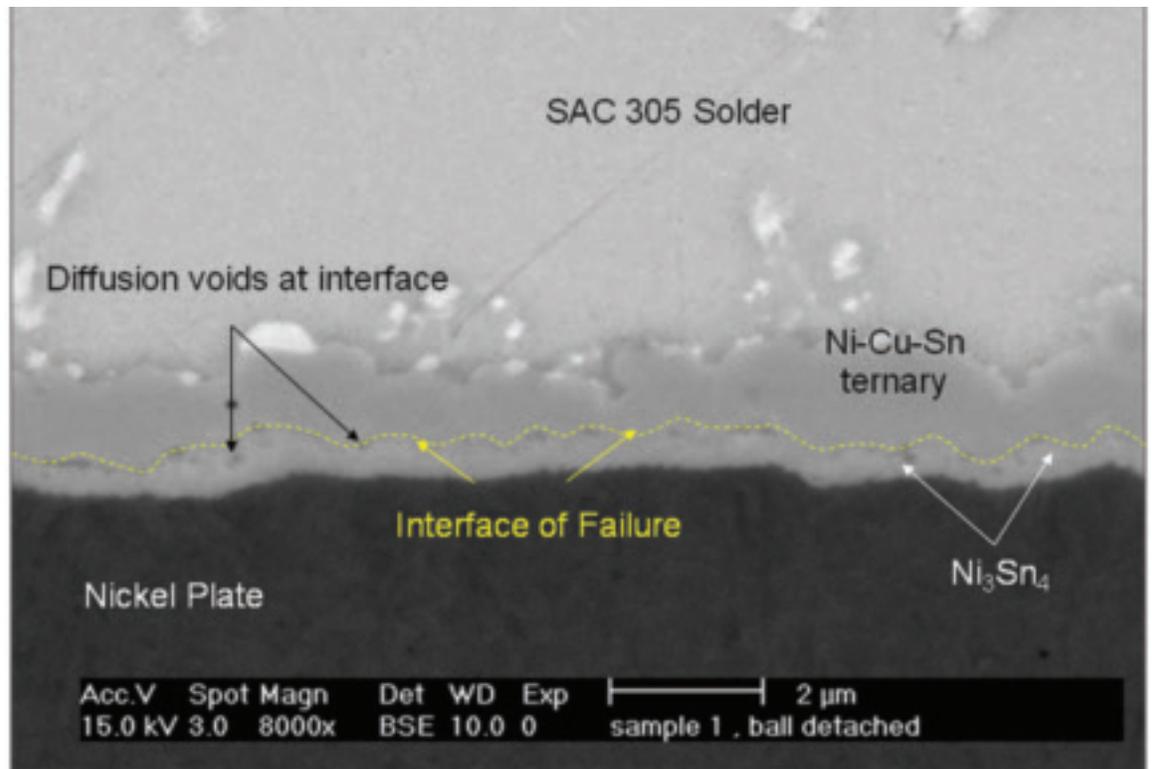


Figure 10: Higher Magnification of IMCs at SAC Ni Interface. The line is drawn as a guide to the eye.

- Ternary IMC compounds, where reacting atoms are incorporated in the IMC structure substitutionally, have degraded mechanical, thermal and electrical properties relative to binary compositions due to imposed lattice strain from the atomic substitution. In this case, failure can occur within the ternary compound (as in the AuSn example) or at the interface between a binary and ternary IMC (as in the case of the SAC example).
- By implication, steps to minimize the extent and thickness of IMCs are key to improving package reliability.

As is clear from this article, completely eliminating formation of IMC at interfaces is not a practical solution for most applications. However, there are some

actions that can be taken to try to minimize the reliability issues associated with IMC formation.

- **Microstructural Characterization:** It is very important to understand the microstructure of all interfaces, including the identity and morphology of any IMC phases. This is best accomplished utilizing cross-sectional SEM analysis. Interfacial microstructure as a function of processing conditions is very valuable for minimizing IMC impact.
- **Failure Mechanism Identification:** Determining how and where interfaces fail is critical information for gauging reliability. For example, single mode interfacial failure, even at a high induced stress level, raises concerns because it indicates the interface is the “weakest link.” Since external

stresses usually concentrate at interfaces, this type of failure mode may impact reliability.

- **Slow IMC Formation through Alloying:** Doping of plated nickel with cobalt to slow the formation of nickel-silicide IMC phases is a good example of this process. For this example, reliability of the die attach was greatly improved through this approach.
- **Minimize Diffusion Effects:** To form a thick, continuous IMC layer at an interface in some cases requires significant solid state diffusion. This is most often seen in “aging” studies, when a thin IMC layer may grow thicker, and thus more influential, when the material is exposed to long temperature cycles. This phenomenon has been studied by Zribi et al. for PbSn solders (see Reference iv). Diffusion effects in this situation can be minimized by limiting thermal exposure. Potential IMC growth should also be considered when determining acceptable thermal budget specifications.
- **Minimize Concentrations of IMC Constituents:** This approach has been used for many years to minimize AuSn IMC formation in the case of PbSn soldered to a gold plated pad. By minimizing Au thickness to the very minimum required for oxidation resistance, the extent of AuSn formation is mitigated.

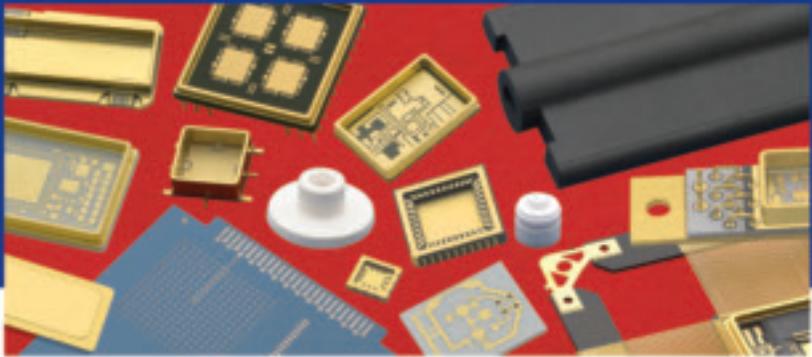
- **Solder Selection:** Choice of appropriate solders for a specific application is also critical. For example, the use of Cu containing solder on Ni underplate can lead to ternary Cu-Ni-Sn IMC formation. Use of a Ag-Sn solder would avoid this issue.

#### References

- i Binary Alloy Phase Diagrams, Thaddeus Massalski, ed., 2<sup>nd</sup> Edition, ASM, 1990
- ii R.J. Fields and S.R. Low, NIST Metallurgy Division, Research Publication
- iii See, for example, J.H. Harris and E. Rubel, Semiconductor International, September 2007
- iv Zribi et al., 1999 ECTC Proceedings, IEEE, 451

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The process of identifying deserving nominees, and submitting and reviewing the nominations is very thorough. Most awards are reviewed by past recipients, making these awards the recognition of notables by notables. We encourage all IMAPS members to nominate those notable for consideration of an award by August 15, 2008. The awards presentation will be on Tuesday, November 4, 2008, preceding the Symposium's keynote speaker.

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The two students winning the competitions receive a cash prize of \$1000. IMAPS will also pay for travel expenses and registration to the respective advanced technical workshops. These winning students will also gain recognition at the workshop and in IMAPS publications.

## HiTEC Competition:

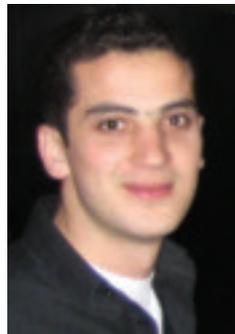
- **Winner:** Mr. Pedro Quintero, University of Maryland
- **Advisor:** Professor F. Patrick McCluskey (McCluskey is also his advisor)
- **Paper Title:** High Temperature Die Attach by Transient Liquid Phase Sintering
- **Co-Author:** Timothy Oberc
- **Bio:**



Pedro Quintero received a BS and MS in Mechanical Engineering from the University of Puerto Rico. After his graduate degree, he joined the electronic industry in 1997 working as a process engineer for Intel Corporation. Pedro joined Hewlett Packard in 2000 where he served as a Member of the Technical Staff for the second-level interconnection process. He started his Ph.D. training in 2005 at the University of Maryland working for the CALCE research center. He is currently a PhD candidate working on the development of die attach for high temperature environments using transient liquid phase sintering methods.

## Advanced Substrates and Next-Generation Semiconductors Competition:

- **Winner:** Mr. Shadi Dayeh, University of California, San Diego
- **Advisor:** Professor Deli Wang and Professor Edward T. Yu
- **Paper Title:** Integration of Vertical and Electrically-Isolated III-V Nanowires on Insulator on Silicon
- **Co-Authors:** Yi Jing, Peng Chen, Edward T. Yu, Deli Wang, and S. S. Lau
- **Bio:**



Shadi Dayeh joined the PhD program at UCSD. His main research work is on the growth, fabrication, and characterization of III-V semiconductor nanowires; particularly InAs nanowires, in which he made marked contributions in both areas of its growth and devices. Shadi is also very involved in academic service at UCSD. He works as a lead teaching assistant consultant for the sciences and engineering departments where he has initiated and conducted the new ECE TA training program. Shadi was selected in 2007 as the Summer Graduate Teaching Fellow for the ECE department in which he has taught ECE103, Fundamentals of Devices and Materials.

## In Memoriam – Bob Waer

We are sad to report that one of our Founding Fathers, Bob Waer, passed away on January 3, 2008. Bob was one of the four who first began ISHM, now IMAPS. He was a featured guest at our 40<sup>th</sup> Annual International Symposium in San Jose. We were all pleased to be able to meet him and to acknowledge his great service to our Society and show him how far we have come since 1967. We are thankful that he was part of our beginning.

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## Angel Chapter

The IMAPS Angel Chapter held its SoCal'08 Technical Symposium and Tabletop Exhibition on June 4. This one-day symposium featured complimentary admission, lunch, over 25 exhibitors, and 12 presentations. The presentations and exhibits covered the technical areas of military, aerospace, space, commercial microelectronics, and electronics packaging.

For more on So Cal 2008 and other Angel Chapter meetings, please view [www.imaps/chapters/angel](http://www.imaps/chapters/angel)

## Arizona Chapter

The IMAPS Arizona Chapter held a member luncheon, tour, and presentation at the Flexible Display Center at Arizona State University on April 17. Dr. Doug Loy and Dr. Shawn O'Rourke, directors at the Center, gave an overview of materials and processing challenges associated with display manufacture on flexible substrates to 25 Arizona chapter members. The high level discussion focused on materials and processing necessary for the temporary bonding and debonding process, the approach to lithography on warped substrates, and the thermal restrictions associated with processing on plastic. Following the talk, the Center's staff provided a 20-minute tour of their facility and manufacturing capabilities.

## Florida Chapter

The IMAPS Florida Chapter's June meeting featured a reception, dinner, and presentation on LTCC by Michael Ehlert, Director of Process Engineering of Barry Industries Inc. Mr. Ehlert is also the IMAPS First Past President. Mr. Ehlert provided a broad overview of LTCC from conception to the present. He examined some of the key drivers for its conception, what makes it unique, and possible future applications. Mr. Ehlert later reported on the latest status on the current work in developing a comprehensive set of standards for all branches of the LTCC supply chain including fired properties, un-fired properties, and processing. For more information, please view <http://www.imaps.org/chapters/florida/index.htm>.

## Indiana Chapter

### IMAPS Indiana's 2008 Vendors Day and Technical Symposium

The IMAPS Indiana Chapter held its 23rd annual Vendors Day and Technical Symposium in Indianapolis on April 14, 2008. The event featured 53 attendees, 15 vendor tables, and 8 technical presentations. Eighteen door prizes from the chapter, IMAPS, and several participating vendors were provided.

Presentation topics included computed tomography, embedded dielectric capacitors in LTCC substrates, component reliability, RoHS compliance, and electrically conductive adhesives. Of special interest to attendees was Delphi Electronics' concept vehicle for information, convenience, and protection. Dr. William Chappell of Purdue University won the Best Paper award for his presentation, "Advancements in Tunable Front Ends for Wireless Systems."

The event marked the conclusion of a successful 2007-08 meeting schedule in which Indiana IMAPS witnessed the past, present and future of manufacturing in the state of Indiana. These past meetings included tours of Haynes International in Kokomo (nickel and cobalt-based alloys), the Studebaker Museum in South Bend, DePuy Orthopedics in Warsaw, and Wabash National (semi trailers) in Lafayette. The IMAPS Indiana Chapter will continue to focus on Indiana manufacturing during the meetings and tours in 2008-09.

Please see <http://www.imaps.org/chapters/indiana/index.htm> for more information.

## New England Chapter

### IMAPS New England Chapter Symposium & Expo

The IMAPS New England Chapter held its 35th Symposium and Expo on May 6th with the sport theme, "Champion Nation." This show was a great success with over 80 exhibitors and nearly 500 attendees.

The technical symposium included session topics on ceramics, cavity plastic packaging, surface mount technology, optoelectronics, microwave, and thermal management. The poster sessions included good student presentations from Worcester Polytechnic Institute, University of Massachusetts-Lowell, and SUNY-Binghamton.

This successful symposium illustrates the important role of New England area businesses and universities in electronics development and innovations. The IMAPS New England Chapter provides a vital link to the multiple disciplines that are necessary for these innovations.

Planning is underway for next year's 36th Symposium and Expo to be held May 5th 2009. For more information and pictures from this year's event, please visit [www.imapsne.org](http://www.imapsne.org).

## April Meeting

For its April monthly meeting, IMAPS New England members toured the plant of Stellar Industries. Over 30 chapter members gained information on Stellar's custom lapped and polished electronic grade ceramics and custom services for metallizations on these ceramics. For more event pictures, tour information and a PowerPoint presentation, see <http://www.imapsne.org/lastmeeting.html>.



L-R: Eric Brown, John Snook, Derek Richardson, and Wendy Sherwood

## AMERICAN CHAPTER NEWS

### Viking Chapter

IntriCon Corporation hosted the IMAPS Viking Chapter meeting on April 10, 2008. The meeting featured tours of the IntriCon electronic assembly facility in Arden Hills, MN and the IntriCon micro-miniature insert molding facility in Vadnais Heights, MN.

Chris Conger, Vice President of Engineering at IntriCon, presented two case studies at IntriCon. The first was a fast-track program for design and manufacturing in a clean room environment for a medical application. The second case study was how IntriCon brought back an offshore medical program to the USA through the use of automation and superior quality systems.

Planned events for the Viking Chapter for 2008 can be seen on the chapter web site at <http://www.imaps.org/chapters/viking/index.htm>.



Viking Chapter meeting at IntriCon Corporation

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**France:**

**Meetings Program:**

**Technical day “Connectique” Paris, October 23**

The next 1-day technical meeting of IMAPS France will be held, October 23, in the conference rooms of the Novotel, Paris La Défense.

Entitled “Journée Connectique,” it will be dedicated to the new connection challenges in different fields of application.

Innovative connection devices or traditional connectors, specific technologies for microwaves or optics, the connection solutions will have to follow the requirements of the different market sectors.

- Miniaturization for customer mobile products.
- Increasing high rate for the multimedia telecommunications and the data transmission needs related to the new system architectures.
- Power, environment stresses and electromagnetic compatibility for automotive, including the new hybrid and electrical vehicles.
- High reliability for the military, aerospace and medical fields.

The assembly solutions, on printed circuit board as well as on flexible printed circuit, will be included too in the program.



**News from the Chapter:**

**Thanks to our webmaster**

Jean-Louis Fouré will not renew his mandate as board officer and webmaster of IMAPS France.

We want here to congratulate him for his work on the board and particularly for the design and maintenance of the French site as well as for his contribution to the European one.

Many thanks, Jean-Louis and good luck in your new activities.

**IMAPS France web site**

For the incoming events, the site is progressively updated by our webmaster with the useful documents as soon as available: Poster, Call for papers, Exhibitors files, Technical program, Registration files.

The “member only” section is open to our members with their membership number as a password. Besides the directory of IMAPS France, papers presented at IMAPS events are available on line.

Visit us @: [www.imapsfrance.org](http://www.imapsfrance.org)

Links are available for a direct access to other chapters in Europe and United States.

**More information?**

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**Germany:**

**Meetings Program:**

**Autumn Conference, October 14-15, Munich**

The yearly autumn conference takes place at the Technical High school, Munich.

More info on [www.imaps.de](http://www.imaps.de)

**News from the Chapter:**

**CICMT 2008, Munich, April 21-24**

More than 75 papers, 50 posters, 31 exhibitors attracted 250 delegates to the very well organized event at Holiday Inn in Munich. The choice of venue was perfect with very good conditions for exhibitors, with two adjacent conference rooms and space for good logistics regarding the serving of lunches and the coffees. To this comes a fair price of the hotel rooms and a good location near the subway with access to the center city or airport.

If anybody had had the impression that ceramics technologies were fading away and lost attraction, the conference demonstrated the opposite. Not only for harsh environments and high end products in the automotive, space and military sector but also in high volume mobile phone applications, thickfilm or LTCC will or can be the solution. But it is not an easy task to “sell” these technologies to the design engineers who most often prefer the “easier” solutions on laminate substrates due to the well established design rules and larger formats. System cost issues have to be addressed and it would be nice if cost benefits via high(er) reliability, less service, better thermal management could be seen more clearly, when cost comparisons between technologies are made.

Anyway, the organizers had done what they could to create an ideal ambience for the visitors to CICMT with sufficient time in the breaks to network and with the social arrangements for getting together.

A few pictures also from the gala dinner in a beer cellar illustrate this.

SN



Break

## Announcement IMAPS Advanced Technology Workshop on Thermal Management

**The Cabaña Hotel & Resort (A Crowne Plaza Resort)  
Palo Alto, California - USA  
October 14 - 16, 2008**

*Sponsored by*  
**International Microelectronics And Packaging Society (IMAPS)**  
**Bringing Together the Entire Microelectronics Supply Chain!**

**ABSTRACT DEADLINE: JULY 30, 2008**

<p style="text-align: center;"><b>General Chair:</b> Dave Saums, <i>DS&amp;A LLC</i> Amesbury, MA - USA Email: <a href="mailto:dsaums@dsa-thermal.com">dsaums@dsa-thermal.com</a> Tel: 978-499-4990</p>	<p style="text-align: center;"><b>Program Chair:</b> Vadim Gektin, <i>Sun Microsystems, Inc.</i> Santa Clara, CA USA Email: <a href="mailto:vadim.gektin@sun.com">vadim.gektin@sun.com</a> Tel: 408-276-6580</p>
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This workshop is organized each year by IMAPS to promote discussion of leading-edge developments in thermal management components, materials, and systems solutions for removing, spreading, and dissipating heat from microelectronic devices and systems. The Workshop emphasis is for *practical, high-performance solutions* to meet current and evolving requirements in computing and wireless/telco systems. Single-company product development concepts are acceptable subjects; however, all abstracts will be judged on novel and innovative contributions to the industry knowledge.

This Advanced Technology Workshop (ATW) on Thermal Management has been held since 1992 and is considered to be one of the most successful of the IMAPS ATWs that are held each year. The 2007 Workshop featured 35 presentations, eight of which were competition-selected graduate student papers. The hotel at 4290 El Camino Real in Palo Alto, CA, was renovated in 2007. Information will be available on transportation methods by train and/or bus from area airports.

Speakers are required to attend the entire Workshop to maximize opportunities for interaction with registered attendees. All authors and attendees find that this IMAPS Workshop format is a proven forum for informal but highly effective networking between attendees and speakers. Speakers are required to pay a reduced registration fee.

### ABSTRACTS ARE SOLICITED IN THE FOLLOWING AREAS:

- ◆ **Market Drivers:** Thermal challenges and drivers combined with market trends, market segment size, cost drivers, and performance and reliability requirements.
- ◆ **Thermal Interface Materials and Testing:** Developments in thermal materials for high-performance processors, memory, and wireless/telco components and systems. Standards for reliability and testing. Metallic, metal matrix and polymer matrix materials.
- ◆ **High Conductivity Materials:** Metallic, ceramic and other composite materials with thermal conductivity equal to or higher than aluminum or copper, as well as thermal expansion closer to that of silicon and ceramic.
- ◆ **Device Packaging:** Chip-level packaging, including System-On-Package, Multi-Chip Module and Multi-Package Module, thermal/interconnect concerns.
- ◆ **Liquid and Phase-Change Cooling:** Advances in alternative solutions as well as reliability, serviceability, and availability.
- ◆ **Refrigeration Cooling:** Presentations on advances in alternative solutions as well as reliability, serviceability, and availability.
- ◆ **System Cooling:** Component- and system-level thermal management solutions for high-performance computing systems.
- ◆ **Data Center Cooling:** Studies of cooling provisioning, airflow and temperature distribution, and migration paths from air to liquid cooling.
- ◆ **Military and Aerospace Apps:** Thermal management of legacy, emerging, and future military and airborne components and platforms.
- ◆ **Telecommunications Systems:** Component- and system-level thermal management solutions for high-performance telecommunications systems.
- ◆ **Consumer Electronics:** Component- and system-level thermal management solutions for stationary and mobile systems, including displays, desktop and notebook computers, and handheld devices.

### PREPARATION OF ABSTRACT:

Speakers should submit one copy of a two-paragraph abstract describing their proposed 25-minute presentation **no later than July 30, 2008**. No formal technical paper is required. A reproduction-ready two- to six-page concise summary with text (figures and graphs included if necessary) will be required for the abstract booklet on Friday, September 12, 2008. A post-conference CD containing the full presentation material as supplied by authors will be mailed 15 business days after the event to all attendees.

Abstracts must be submitted on-line at <http://www.imaps.org/abstracts.htm>.

Contact Jackki Morris-Joyner with questions: [jmorris@imaps.org](mailto:jmorris@imaps.org) or 305-382-8433. You may also contact the workshop chairs.

Official workshop site: [www.imaps.org/thermal](http://www.imaps.org/thermal)

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Exhibition



Committee



Beer Barrel



Dinner

*More information?* On IMAPS Germany? Events? Latest CD ROM proceedings? Membership? Please contact:  
www.imaps.de  
Martin Oppermann, Point of Contact AM,  
martin.oppermann@imaps.de

## Hungary:

### News from the Chapter:

ISSE 2008, Spring Seminar, May 7-10

This 31<sup>st</sup> International Spring Seminar on Electronics Technology attracted 160 delegates and had 140 oral and poster presentations.

Again this European event had high focus on bringing people together after the technical sessions.

The full arrangement package gave also the delegates from the many countries outstanding sightseeing possibilities with opening reception at the Technical University, a dinner during a cruise on the Danube, an excursion to a castle and an organ concert in Gödöllő with outdoor dinner at a Czardas restaurant with folkloristic entertainment and finally a Gala Dinner where various awards were exchanged.

Many thanks to Prof. Zsolt Illyefalvi-Vitéz and his team for hard work and a very interesting event.

Some pictures illustrate the experience.

SN



Budapest



ISSE Opening



Excursion



Folklore

**Italy:**

**Meetings Program:**

EMPC2009, Rimini, June 14-17, 2009

The IMAPS Steering Committee has started the implementation of the EMPC2009 conference with exhibition.

It will take place June 14-17, 2009 at Rimini, a beautiful tourist spot on the Adriatic Sea in the north-east side of the country.

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# From slurry to sintering, count on Harrop.

**Engineered equipment for processing  
thin film and ceramic tape**



**Carsten  
Tape Casters**

The Carsten line of lab and production models feature automatic slurry control with micrometer adjustment to within 0.0001" of wet tape thickness. PLC temperature controlled multi-zone infrared and forced air heating, self-aligning belt drive, and enclosed cabinet for cleanliness. Caster lengths from 6 ft. to more than 100 ft.

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Call Rimini

The Call for papers are now available at [www.empc2009.org](http://www.empc2009.org).

Please check the website and read about Rimini, find the exhibitor details, etc. Enjoy!

**News from the Chapter:**

*More information?* For more information on IMAPS Italy and its events, please look at: [www.imaps-italy.it](http://www.imaps-italy.it) or [www.italy.imaps.org/](http://www.italy.imaps.org/)

**Nordic:**

**Meetings Program:**

IMAPS Nordic 2008, Hotel Marienlyst, Helsingoer, Denmark, September 14-16

The 2008 event takes place in Denmark. Again the well suited and popular Hotel Marienlyst, Helsingoer, located at the beach and close to the Kronborg castle, has been chosen. Kronborg is world famous as the home of prince Hamlet.

The exhibition area is located just outside the conference rooms allowing and encouraging maximum interaction.

The conference will focus on both the latest most exotic and new topics (SIP, TSV, stacking, thinning, embedding, etc.) as well as on the day-to day challenges, manufacturing and system cost issues.

Please mark the dates in your calendar now.

The Program and Exhibitor package is available at <http://www.imapseurope.org/nordic/Past.asp>

More info: please mail [info@imapsnordic.org](mailto:info@imapsnordic.org)

**News from the Chapter:**

*More information?* On IMAPS Nordic? Events? Membership? Please check the IMAPS Nordic homepage at <http://www.nordic.imaps.org/>

**Poland:**

**Meetings Program:**

IMAPS Poland – September 21-24

The 32<sup>nd</sup> IMAPS-Poland International Conference, September 21-24, will take place in The Polonia House in Pultusk (60km from Warsaw). Chairman of the Organizing Committee is Malgorzata Jakubowska. For further details, please check <http://imaps2008.imio.pw.edu.pl>, [www.poland.imaps.org/index.asp](http://www.poland.imaps.org/index.asp) or contact: Malgorzata Kramkowska, [malgorzata.kramkowska@pwr.wroc.pl](mailto:malgorzata.kramkowska@pwr.wroc.pl)

**UK:**

**Meetings Program:**

ESTC 2008, September 1-4, Greenwich

The IEEE ESTC Electronics Systems-Integration Technology Conference (ESTC) is the Major Electronics packaging, interconnection and integration conference of Europe held biennially. ESTC alternates with the IMAPS European Microelectronics Packaging Conference and is co-sponsored by both IEEE-CPMT and IMAPS-Europe. This second ESTC to be held during 1<sup>st</sup> – 4<sup>th</sup> September 2008 follows the very successful first ESTC held in Dresden in 2006.

ESTC-2008 will be held at Greenwich, the magnificent World Heritage site and major maritime site on the banks of the River Thames in the great city that is London. The Conference and Exhibition will be hosted at the University of Greenwich in the buildings of the former Royal Naval College – which has a tremendous heritage: Plenary sessions will be in the Great Painted Hall – providing a wonderful ambience for the technical presentations; and when you visit the Exhibition you will be standing directly over the former palace of King Henry the Eighth, and the Queens House is where Sir Walter Raleigh placed his cloak over a puddle for Queen Elizabeth the First to step onto.

More on: [www.estc.biz](http://www.estc.biz)

## IMAPS Advanced Technology Workshop and Tabletop Exhibition on Photovoltaics, Fuel Cells and other Emerging Technologies in the Development of Alternative Energy

[www.imaps.org/energy](http://www.imaps.org/energy)

*Hotel Albuquerque at Old Town  
Albuquerque, New Mexico - USA  
August 12 - 14, 2008*

*Due to scheduling challenges with the IMAPS Energy event and other local energy-related meetings in the New Mexico region this spring, IMAPS has decided to reschedule Alternative Energy 2008. The event will now be held August 12-14, 2008, still at the Hotel Albuquerque in New Mexico.*

The **Advanced Technology Workshop and Tabletop Exhibition on Photovoltaics, Fuel Cells and other Emerging Technologies in the Development of Alternative Energy** will be held at the Hotel Albuquerque at Old Town, Albuquerque, New Mexico. It is being produced by the International Microelectronics And Packaging Society (IMAPS). This conference is a continuation of last year's first Alternative Energy Conference. It will focus on this critical field that will be affecting every aspect of our lives worldwide. Core issues involve both new technologies, and materials/processes for renewable, non-renewable, and innovative application of existing technologies. Incentives for research, investment, and adoption are already practiced in some Asian and European countries. Following new energy policies in the US and other countries, these incentives are now available to encourage the adoption, research, and development of new technologies.

### **SESSIONS ARE BEING CREATED IN THE FOLLOWING AREAS:**

Solar - Photovoltaics  
Fuel Cells  
Geothermal  
BioFuels  
Batteries and Hybrids  
Wind

Other Approaches  
Thermal and Power Management  
Inverter Materials and Design  
Grid and Storage Approaches  
Design for Efficiency  
Materials & Reliability

Qualification Approaches  
Environmental Regulations  
Government/State Policies and  
Incentives

**A tabletop exhibit is planned for Tuesday, August 12<sup>th</sup>; 12:00 noon - 7:30 pm.  
Contact Ann Bell at [abell@imaps.org](mailto:abell@imaps.org) or 202-548-8717 for information  
about tabletop exhibits.**

**Details will be posted on the website at [www.imaps.org/energy](http://www.imaps.org/energy).**

## Announcement and Call for Abstracts

### Advanced Technology Workshop and Tabletop Exhibit on **Printed Devices & Applications**

[www.imaps.org/printed](http://www.imaps.org/printed)

**February 25 - 27, 2009**  
International Plaza Resort  
10100 International Drive  
Orlando, Florida 32821

**Abstract Deadline: November 21, 2008**

<b>General Chair:</b>	<b>Printed Devices &amp; Applications Workshop Organizing Committee:</b>		
<b>C. Mike Newton</b> P: 321-729-3748, <a href="mailto:mnewton@imaps.org">mnewton@imaps.org</a>  <b>Technical Chair:</b> <b>Dr. Ken Church - nScript</b> P: 407-275-4720, <a href="mailto:kchurch@nscriptinc.com">kchurch@nscriptinc.com</a>	Carol Gamlen	Harris Corp.	<a href="mailto:cgamlen@imaps.org">cgamlen@imaps.org</a>
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	Mike Hudgens	Corwil	<a href="mailto:mhudgens@corwil.com">mhudgens@corwil.com</a>

#### **Printed Devices & Applications Workshop Focus:**

The objective of the Printed Devices Workshop is to provide a unique forum that brings together scientists, engineers, manufacturing, academia, and business people from around the world who work in the area of printed electronics as an emerging packaging technology. This workshop enables discussion and presentations on the latest materials, process, design & emerging applications of printed electronics technology.

- Digital Printing / Deposition Technologies
- Nanomaterials, inks & epoxies
- Printed devices – Active and passive
- Thin & printable battery technology
- Membrane and capacitive switches
- Novel die interconnect
- Paper based, PET & PVC substrate media
- Printable display & lighting
- Antennas
- Design, Simulation and Modeling
- Applications and new markets
- Convergence of Graphics & electronics

Those wishing to present a paper at the Printed Devices & Applications Advanced Technology Workshop must submit a 200-300 word abstract electronically **no later than November 21, 2008**, using the on-line submittal form at: [www.imaps.org/abstracts.htm](http://www.imaps.org/abstracts.htm). Full written papers are not required; however, an extended abstract of 1-4 pages is due for accepted presenters no later than January 23, 2009.

Please contact Jackki Morris-Joyner by email at [jmorris@imaps.org](mailto:jmorris@imaps.org) or by phone at 202-548-4001 if you have questions.

Accepted papers may be considered for publication in the IMAPS *Journal of Microelectronics and Electronic Packaging*. **All Speakers are required to pay a reduced registration fee and are required to attend the entire event.**

[www.imaps.org/printed](http://www.imaps.org/printed)

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# IMAPS 2008

## Providence, Rhode Island

### November 2-6

IMAPS will be holding the 41<sup>st</sup> International Symposium on Microelectronics in November in Providence, RI with technical sessions addressing everything in packaging “*between the chip and the system.*” You will find distinct benefits by attending this year’s conference through gains in understanding the newest technical challenges we all face in electronic product enhancement for the global marketplace. In keeping with the international nature of this conference and to reflect globalization of the electronics marketplace, translated Japanese and Chinese sessions will again be included in our agenda. This year’s show will focus on biomedical, telecom, military, consumer electronics, and for the first time, alternative energy applications. We will continue to demonstrate the importance of System Packaging/Applications/Design with software and firmware applications through a series of design sessions. Imaging sensors and their continued increased packaging requirements will be included as last year. ESD protection, packaging for extreme environments, ceramic, polymer and conductive materials, and microwave communications are again planned for 2008 as these session topics are of profound importance as design constraints continue to shrink and more electronics find homes in severe environments. The New England area is rich in IMAPS-related companies and technology and we are particularly excited this year that the symposium is in Providence, RI. This area is a hot-bed of technology investors and we fully expect a lot of attendance from many of these new companies. The technical program will consist of 6 parallel sessions addressing these topics during the symposium as well as 16 Professional Development Courses (PDC). We look forward to seeing new and current members at our technical sessions in Providence. Come ready to learn about your area of expertise, aid others in learning about your subject, and network with past and new business associates.

Jim Drehle and Kishio Yokouchi are gathering the presentations for another Japanese translated session and Randy Kline and Charles Luo are similarly preparing one Chinese translated session. Both sessions will delineate the technical advances in the technology in their countries and offer a great learning experience to all attendees.

Sponsorship is an integral part of such a large undertaking. To date, we are fortunate that our platinum – Natel Engineering, gold – Panasonic Factory Solutions, and silver – Hesse & Knipps sponsors have all agreed to help us again this year. SEFAR is repeating as the Badge Holder Lanyard sponsor and Umicore has joined our list at the \$10,000 level. Thanks to all of them for their support. There are several other opportunities to sponsor still available; contact [abell@imaps.org](mailto:abell@imaps.org). The exposure provided by IMAPS

makes being a sponsor a very viable advertising technique.

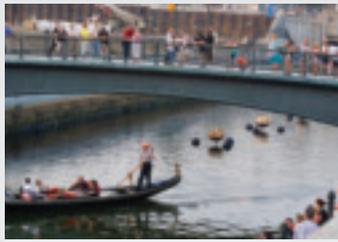
We are working hard to bring 220 exhibitors to the event and to date 135 booths have been sold. This event will fill up quickly, so if you plan to exhibit you should contact Ann Bell at headquarters soon. Area Military Contractors include Lockheed Martin, BAE, Northrop Grumman, Harris, Sakorsky, Raytheon, United Technologies, Martin Marietta, Draper Labs, Concord Labs, and Allied Signal. Also headquarters for Analog Devices, GE, IBM, Honeywell, Raytheon, Xerox, Kodak, L-3, Textron, EMC, Fisher Scientific, Corning, Raytheon, Boston Scientific, and GTE are in the Providence area. The NE area is rich in Microelectronics, so don’t miss this opportunity to exhibit at this event.

The 2008 Companion Tour will occur on Tuesday, November 4 and Wednesday, November 5, with visits to Mystic, CT, and Newport, RI. Newport’s 11 historic mansions and landscapes - seven of which are National Historic Landmarks - trace America’s architectural and social development from the Colonial era through the Gilded Age. Since the 1600s, Mystic Seaport has been a center of shipbuilding. As the great Age of Sail gave way to steamships and railroads, wooden ships and boats were turned into firewood and the nation’s seafaring traditions began to disappear, three Mystic residents decided to work together to keep the past alive. The story of the town’s nautical connection is told at the Mystic Seaport, the world’s largest maritime museum. Look for more information in the IMAPS 2008 Advance Program.

The annual Foundation Golf Tournament will take place on Monday, November 3<sup>rd</sup> at the Alpine Country Club in Cranston, Rhode Island. This is a private, family-oriented country club, rich in tradition as it is in natural beauty. Home of one of New England’s most challenging course layouts, Alpine Country Club has played host to some of Rhode Island’s most time-honored golf tournaments. Nestled on 205 quiet acres, Alpine Country Club is located in the Rhode Island countryside just 5 miles west of historic Providence and can be viewed at [www.alpinecountryclubri.com](http://www.alpinecountryclubri.com). Golf chairs Howard Imhof and Gary Hemphill are working hard to gather sponsors for the event and prices for the players.

Providence has big city amenities and small town charm, easy to get to and to get around with great restaurants, museums and entertainment at your fingertips. We look forward to seeing you at our 41<sup>st</sup> International Symposium in Providence, Rhode Island.

Larry Rexing  
General Chair  
IMAPS 2008 Symposium



# About Providence

Providence, one of the first cities in America (1636), is the capital of the smallest state in the union. This historic city boasts a fascinating blend of colorful history and unusual technologies. The great manufacturing mills, many still standing, played a key role in the American Industrial Revolution that was launched along the many rivers in this region. You can still see, and even touch, some of the massive factory steam engines that are preserved — and operational — at the famous New England Wireless and Steam Museum located 30 minutes south of the city. Providence is home to many metal artisans, and has long been the jewelry manufacturing capital of the USA — an art still practiced, although on a smaller scale. Education was highly valued from the start, and world-renowned Brown University is just a short walk from the Convention Center. The remarkable 131-year old Rhode Island School of Design is also nearby and includes an extraordinary museum. But it is Johnson & Wales Culinary School that insures Providence has the best food in New England.

This ancient historic city, founded by seekers of religious freedom, continues to embrace the newest technologies with passion. Cyber tech, software development, biotech are important pursuits. Rhode Island is also a center for high-tech gaming technology and equipment with GTECH's new headquarters building recently completed in the downtown area. Providence probably has more miles of fiberoptic per capita than any other place in the USA. Today, the area is in the midst of a massive fiber-to-premise rollout that will eventually link the home user to the Internet at a blazing 100Gbit/sec. So come to the Ocean State to enjoy the old, the new and the strange; Providence was also home to horror story pioneer - HP Lovecraft.



*There is a lot going on in Providence!*



**Area Military Contractors: Lockheed Martin, BAE, Northrop Grumman, Harris, Sikorsky, Raytheon, United Technologies, Martin Marietta, Draper Labs, Concord Labs, Allied Signal, DoD**

**New England companies working with Alternative Energy received over \$500 million in venture capital monies last year!**

**Local Engineering Schools include; MIT, Worcester Polytechnic Institute, ASS, Yale, Stevens, Rensselaer, Colgate, Northeastern**

**Headquarters for: Analog Devices, GE, IBM, Honeywell, Raytheon, Xerox, Kodak, L-3, Textron, EMC, Fisher Scientific, Corning, Raytheon, Boston Scientific, GTE**

**Along with the IMAPS 2008:**

**Superb Technical Program  
Professional Development Courses**

**Global Business Marketing Forum  
Japanese and Chinese Translated  
Sessions.**

***Providence has big city amenities and small town charm. It's easy to get to and to get around with great restaurants, museums and entertainment at your fingertips.***

# IMAPS Global Business Council Fall Marketing Forum

Wednesday, November 5 from 5:15 - 6:15

2008 IMAPS International Symposium in Providence, RI

The GBC Marketing Forum is a business session for all IMAPS 2008 attendees.  
A networking reception will follow.

## Alternative Energy: Options, Supply Chains, and Industry Trends

### Confirmed Speakers:

**Mr. Richard Chleboski**  
Strategic Marketing  
Vice President  
Evergreen Solar, Inc.



### “PV Industry and the Challenges of Rapid Growth”

Mr. Chleboski will provide an overview of the solar power industry. The talk will provide a brief overview of the industry’s history, its recent rapid growth and future opportunities. Particular focus will be on the supply chain challenges for an industry that has been growing over 50% annually and what challenges the industry faces to achieve parity with grid power.

### About Mr. Chleboski:

Mr. Chleboski co-founded Evergreen Solar in 1994. He has served in many leadership positions since then. Previously, he worked at Mobil Solar Energy Corporation for seven years where he was the Strategic Planner focusing on developing long-range business plans working with strategic partners. He also served as a Process Engineer responsible for the operation of Mobil Solar’s manufacturing line. Mr. Chleboski received a B.S. in Electrical Engineering from Massachusetts Institute of Technology and an M.B.A. from Boston College.

### About Evergreen Solar Inc.:

Evergreen Solar Inc. is a global innovation leader in developing, manufacturing and marketing photovoltaic modules – the engines of solar electric systems. The company is recognized as one of the brightest rising stars in the solar industry. Evergreen produces solar panels using the company’s proprietary crystalline silicon technology, known as String Ribbon™. For more information, see [www.evergreensolar.com](http://www.evergreensolar.com)

**Ms. Cecilia Aguillon**  
Director, Business  
Development and  
Government Relations  
Kyocera Solar, Inc.



### “Policies and Incentives to Develop the Solar Industry”

Ms. Aguillon will speak about the roles of government and private sectors in encouraging the growth of solar energy markets in Asia, Europe, and North America. The presentation will describe policy tools used to create incentive programs that are attracting investment, technology improvements, cost reductions, and how solar markets are being shaped by those policies.

### About Ms. Aguillon:

Cecilia Aguillon works with local, state, and federal governments across the United States, Canada, and Mexico on designing and implementing solar energy policies to create robust and sustainable solar markets. She also works with Solar Energy Industry Association Chapters in several states to develop sustainable solar markets. Cecilia graduated with a Master’s degree in International Relations/Pacific Studies from University of California, San Diego in 1998.

### About Kyocera Solar, Inc.:

Kyocera Solar, Inc. serves the widely varying needs of customers for distributed solar electricity through two major market channels. Industrial customers (such as original equipment manufacturers, government organizations, utilities, corporate clients and institutions) are served directly with fully integrated system packages. KSI also serves a global network of Authorized Distributors and Dealers with components, packaged systems, engineering, technical support, and project management. The company’s expertise is based upon designing, manufacturing, and installing the most technologically advanced solar electric power systems available today. For more information, see [kyocerasolar.com/](http://kyocerasolar.com/)

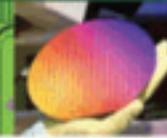
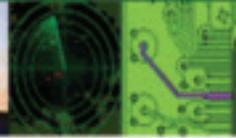
### GBC Forum Chairs:

Howard Imhof, Metalor Technologies USA and Arne Knudsen, Kyocera America, Inc.



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# 2008 IMAPS Student Symposium Programs

## 41st International Symposium in Providence, RI

Take advantage of valuable student programs at IMAPS 2008. These programs are designed to provide technical information, industry insight, and valuable connections.

### Student Paper Competition

Student authors will deliver presentations throughout the Symposium. Their presentations will be evaluated on technical content, presentation skills, the written manuscript, and audience interaction. Winning students will receive cash prizes, a certificate, and recognition in Advancing Microelectronics magazine.

### Student Booth Competition

Students will learn what other academic programs are doing at the student booths. Student booths will be evaluated by a panel of judges on various criteria. Winning chapter booths will receive cash prizes, certificates, and magazine recognition.

### Student Chapter Meeting

Gain more insight and share your success on increasing membership and producing better programs with other student chapter leaders. Learn ways to gain more funding.

### Student-Industry Panel and Reception

The Student-Industry Panel will provide students both career development and industry insight from leading professionals. Industry leaders and professional engineers will describe and discuss how their education, interests, and career experiences led to successful careers. A reception will immediately follow where students will have the opportunity to talk with industry panelists and other leaders.

### Plant Tour: Barry Industries

This industry tour is designed to provide you with industry insight and technical expertise. Barry Industries is a vertically integrated, microelectronics manufacturing company. Barry's product lines are thick film resistor products (precision resistors, power terminations, attenuators - up to 1500 watts pulsed power) and LTCC. The tour will include a guided walk through the facility's areas of design and simulation, the machine shop, CO2 Laser Machining, thick film printing/firing, YAG Laser trim, assembly, and engineering/testing. A valuable group discussion will follow.

### Employment Center

The Employment Center will offer job seekers valuable complimentary services. Center volunteers will post job openings, collect and forward resumes for these postings, and help schedule interviews at the employer's request.

# IMAPS Advanced Technology Workshop on RF and Microwave Packaging

[www.imaps.org/rf](http://www.imaps.org/rf)

**September 16-18, 2008**

The Crowne Plaza San Diego  
2270 Hotel Circle North  
San Diego, CA 92108-2810

*IMAPS SoCal Golf Tournament the morning of September 16, 2008*

## Organizing Committee:

<b>General Chair:</b> Ken Kuang Torrey Hills Technologies, LLC kkuang@torreyhillstech.com	<b>Technical Co-Chair:</b> Franklin Kim Kyocera America, Inc. franklin.kim@kyocera.com	<b>Technical Co-Chair:</b> Sean Cahill BridgeWave SeanC@Bridgewave.com
<b>Advisory Committee</b> (alphabetical order):		
Steve Adamson, Asymtek, Inc. Mumtaz Bora, Kyocera Wireless Corporation Ron Barnett, Giga-tronics/Ascor Incorporated Carl Edwards, Space Micro, Inc. Mark Eblen, Kyocera America, Inc. Aicha Elshabini, University of Idaho Murat Goksel, Space Micro, Inc. Bill Ishii, Torrey Hills Technologies, LLC	Guosheng Jiang, China Central South University Wally Johnson, Coorstek, Inc. Ho Young Kim, General Optechs Iris Labadie, Kyocera America, Inc. Lee Levine, IMAPS VP of Technology Junkun Ma, Southeastern Louisiana University Tricia McGough, Norstar Group Walt Napoleon, KL Marketing	David Shields, Component Surfaces, Inc. Ron Thiel, retired Mark Tomei, Kyocera America, Inc. David Virissimo, SPM Ziliang Wang, Nanjing Electronics Device Institute David Zhang, GTSI Corporation Danny Zhu, Jiangsu Dingqi Sci. & Tech. Co. Ltd

## RF and Microwave Packaging Workshop Focus:

The objective of the RF and Microwave Packaging Workshop is to provide a unique forum that brings together scientists, engineers, manufacturing, academia, and business people from around the world who work in the area of RF and Microwave packaging technologies. This workshop enables discussion and presentation of the latest RF and Microwave technology.

Sessions are being planned in the following areas:

Emerging Technologies	New Design/Materials	New Applications
<ul style="list-style-type: none"> <li>- 60 GHz Personal Area Network (PAN)</li> <li>- Short wave IR packaging</li> <li>- Nanopackaging</li> <li>- 3D RF/MW</li> <li>- New and disruptive technology</li> <li>- EMI shielding for RF/MW packaging</li> </ul>	<ul style="list-style-type: none"> <li>- New power amplifier design beyond LDMOS</li> <li>- Thermal management</li> <li>- New IR sensors without cooling</li> <li>- Plastic RF/MW packaging</li> <li>- Lead free</li> <li>- RF MEMS</li> </ul>	<ul style="list-style-type: none"> <li>- High Power Electronics</li> <li>- Military / Space / Extreme Environments</li> <li>- MEMS/NEMS</li> <li>- Biomedical</li> <li>- Telecommunications</li> <li>- MMIC</li> <li>- Automotive</li> <li>- SIP</li> </ul>

Visit the workshop site for more information, [www.imaps.org/rf](http://www.imaps.org/rf)

## Think Outside the Box ... Sign Up for a PDC

For those of you not familiar with the term PDC it stands for Professional Development Course. Typically a full or ½ day educational seminar taught by an industry expert at an IMAPS event and focused on a specific technology area. The PDC provides the student an opportunity to learn from an expert in a relaxed classroom setting. We all want to be able to “think outside the box”! Attending a PDC is a good first step. With the knowledge gained and valuable peer interaction you may be able to latch onto those one or two really good ideas that make a difference in your company. The PDC experience will change your perspective. In Providence the courses run on Sunday and Monday of symposium week. The PDCs are designed to educate our membership at large and is a primary mission of IMAPS. This year’s PDC selections include some familiar topics covering the basic technology areas along with several new course offerings.

A day or two of professional education is a great way to stay competitive, both from a personal and company perspective. “Enlightened” is how most students feel

after attending an IMAPS-sponsored PDC. Besides the obvious opportunity to learn and grow, attending a PDC is a great way to network. It’s fun to meet and connect with others in the industry, often faced with the same challenges and day-to-day struggles with technology. The PDC experience includes coffee breaks, a nice lunch and social hour at the end of the day to mingle with fellow students and get to know the instructor on a more personal level. All the PDCs include a full set of comprehensive notes for the student and many also include a textbook. Class sizes typically range from eight to thirty students and there is always ample time for questions. The instructors are seasoned professionals hand picked from industry and academia. Many companies require ongoing professional education and the selection offered by IMAPS is a great way to fulfill this requirement.

Sign up now and I’ll see you at the PDCs in Rhode Island!

Tom Green  
2008 PDC Chair

Visit [www.imaps.org](http://www.imaps.org) for links to all upcoming events including:

- ▲ full event descriptions
- ▲ abstract submissions
- ▲ exhibition information
- ▲ event updates



**IMAPS 2008**

**Providence, RI  
November 2-6**

[www.imaps2008.org](http://www.imaps2008.org)

# IMAPS 2008 Exhibitors

As of 6/10/08



- |                                   |  |
|-----------------------------------|--|
| AdTech Ceramics                   | DuPont Electronic Technologies           |
| Advanced Chemical Company         | EFD, Inc.                                |
| Advanced Cooling Technologies     | Emerson & Cuming                         |
| AI Technology, Inc.               | Endicott Interconnect Technologies, Inc. |
| AIM Products                      | Epoxy Technology, Inc.                   |
| ALLVIA, Inc.                      | ES Components, Inc.                      |
| American Beryllia Inc.            | ESL ElectroScience                       |
| American Technical Ceramics       | F&K Delvotec, Inc.                       |
| AMI/Presco                        | Ferro Corporation                        |
| Anaren Microwave                  | Finetech, Inc.                           |
| AOS Thermal Compounds             | FRT of America, LLC                      |
| Asymtek                           | Gannon & Scott                           |
| ASYS Inc.                         | Geib Refining Corporation                |
| Barry Industries, Inc.            | General Metal Finishing Co., Inc.        |
| Bennington Microtechnology Center | GPD Global, Inc.                         |
| CAD Design Software               | Graphite Concepts, Inc.                  |
| Centrotherm Technologies          | GSI Group Inc.                           |
| Chip Supply, Inc.                 | Haiku Tech, Inc.                         |
| Coining, Inc.                     | Harrop Industries, Inc.                  |
| Compex Corp.                      | Heraeus Thick Film Division              |
| CoorsTek                          | Heraeus-SMT                              |
| Co-Planar, Inc.                   | Hesse & Knipps                           |
| CPS Technologies                  | Hi-Rel Laboratories                      |
| Crane Aerospace & Electronics     | Indium Corporation                       |
| Dage Precision Industries, Inc.   | Infinite Graphics, Inc.                  |
| Datacon Technology GmbH           | Innov-X Systems                          |
| Deweyl Tool Company, Inc.         |  |

**IMAPS 2008 Exhibitors...continued**

Interconnect Systems, Inc.

International Manufacturing  
Services, Inc. (IMS)

J-Tech Distributors USA, Ltd.

Kyocera Industrial Ceramics

Kyzen Corp.

Laser Processing Technology, Inc.

Laser Tech, Inc.

Laserod

LINTEC Corporation

Maxtek Components Corporation

Metachem Resins Corporation  
(Merico)

Micro Hybrid Dimensions, Inc.

Micropac Industries, Inc.

MicroScreen LLC

Micross Components Corp.

Minco Technology Labs., Inc.

Mini-Systems, Inc.

Mitsui Chemicals America, Inc.

Miyachi Unitek - Benchmark Div.

NAMICS Technologies, Inc.

NanoDynamics

Natel Engineering Co., Inc.

Newport Corporation

NorCom Systems, Inc.

NTK Technologies, Inc.

NuSil Technology

Oneida Research Services, Inc.

Orthodyne Electronics

Pac Tech USA - Packaging  
Technologies, Inc.

Palomar Technologies, Inc.

Panasonic Factory Solutions Co.  
of America

Paricon Technologies Corp.



**Looking Ahead...**

**IMAPS 2008**

**Providence, RI  
November 2-6**

**IMAPS 2008 Exhibitors...continued**

Perfection Products, Inc.  
 Photofabrication Engineering, Inc.  
 Reactive Nano Technologies (RNT)  
 Reinhardt Microtech AG  
 Reldan Metals, Inc.  
 Remtec, Inc.  
 Riv, Inc. - Thick Film Screens  
 Rogers Corporation  
 SEFAR Printing Solutions, Inc.  
 Semiconductor Equipment Corp.  
 Semiconductor Packaging Materials (SPM)  
 Sikama International, Inc.  
 Silicon Cert, Ltd.  
 Sims Recycling Solutions  
 Sonoscan, Inc.  
 SST International  
 Stellar Industries Corp.  
 Stellar Microelectronics Inc.  
 Taconic  
 TDK Corporation of America  
 Technic, Inc.  
 Technical Materials, Inc.  
 Teledyne Microelectronics  
 Ticona Engineering Polymers

Toray Engineering Co., Ltd.  
 Torrey Hills Technologies LLC  
 Trebor Instrument Corp.  
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Heraeus	Yin Yin	610-825-6050	Yin.yin@heraeus.com	www.heraeus.com	11
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Ticona Engineering Polymers	Steve Cushard	859-372-3164	Stephen.cushard@ticona.com	www.ticona.com	back cover

### Advancing Microelectronics 2008 Editorial Schedule

<u>Issue</u>	<u>Theme</u>	<u>Copy Deadline</u>	<u>Ad Commitment I/Os Deadline</u>
Sep/Oct 2008	IMAPS 2008 Show Issue	July 15, 2008	July 20, 2008
Nov/Dec 2008	Portable and Consumer	Sept. 15, 2008	Sept. 20, 2008

### ...contact IMAPS Headquarters

See staff listing for specific program areas.

## IMAPS HEADQUARTERS

### WHO TO CALL

<b>Michael O'Donoghue</b> , Executive Director, (202) 548-8707, modonoghue@imaps.org, Strategic Planning, Contracts and Negotiations, Legal Issues, Policy Development, Intersociety Liaisons, Customer Satisfaction
<b>Brian Schieman</b> , Director, Program Development and Technology, (202) 548-8715, bschieman@imaps.org, Development of Society Programs, Website Development, Database Management, Communication Tools and other Technology
<b>Ann Bell</b> , Manager, Marketing & Communications, (202) 548-8717, abell@imaps.org, Public Relations, Marketing, Fundraising, Advertising, Exhibits, Advancing Microelectronics
<b>Steve Greene</b> , Membership Manager, (202) 548-8711, sgreene@imaps.org, Member Relations and Services Administration, Dues Processing, Membership Invoicing, Foundation Contributions, Data Entry, Mail Processing, Address Changes, Telephone Support
<b>Rick Mohn</b> , Operations Manager, (202) 548-8703, rmohn@imaps.org, Financial Management, Accounts Payable, Accounts Receivable, Human Resources, Employee Benefits, Budget Issues, Business Services, Facilities Management, Publications Sales
<b>Jackki Morris-Joyner</b> , Technical Program Manager, (305) 382-8433, jmorris@imaps.org, Technical Program Development and Coordination, ATWs, PDCs, Calls for Papers, Speaker Communications, Proceedings Publication, Event Program Activities
<b>Elizabeth Keller</b> , Meetings Coordinator, (202) 548-8716, ekeller@imaps.org

# CALENDAR OF EVENTS

## 2008

### JULY

start	end		
7-14-08	7-14-08	IMAPS/SEMI ATW on Wire Bonding San Francisco, CA <a href="http://www.imaps.org/wirebonding">www.imaps.org/wirebonding</a>	<a href="mailto:imaps@imaps.org">imaps@imaps.org</a>
7-28-08	7-31-08	International Conference on Electronic Packaging Technology & High Density Packaging (ICEPT - HDP) Shanghai, China <a href="http://www.icept.org/newweb/cpage.asp">www.icept.org/newweb/cpage.asp</a>	<a href="mailto:icept2008@fudan.edu.cn">icept2008@fudan.edu.cn</a>

### AUGUST

8-12-08	8-14-08	ATW and Tabletop Exhibition on Photovoltaics, Fuel Cells and other Emerging Technologies in the Development of Alternative Energy Albuquerque, NM USA <a href="http://www.imaps.org/energy">www.imaps.org/energy</a>	<a href="mailto:imaps@imaps.org">imaps@imaps.org</a>
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### SEPTEMBER

9-15-08	9-16-08	IMAPS Nordic 2008 Helsingoer, Denmark <a href="http://www.nordic.imaps.org/past.asp">www.nordic.imaps.org/past.asp</a>	<a href="mailto:conference.nordic@imapseurope.org">conference.nordic@imapseurope.org</a>
9-16-08	9-18-08	ATW on RF and Microwave Packaging San Diego, CA <a href="http://www.imaps.org/rf">www.imaps.org/rf</a>	<a href="mailto:kkuang@torreyhillstech.com">kkuang@torreyhillstech.com</a>
9-22-08	9-23-08	XXXII International Microelectronics and Packaging IMAPS-CPMT Poland Conference Pultusk, Poland <a href="http://imaps2008.imio.pw.edu.pl">imaps2008.imio.pw.edu.pl</a>	<a href="mailto:imaps2008@imio.pw.edu.pl">imaps2008@imio.pw.edu.pl</a>

### OCTOBER

10-14-08	10-16-08	Advanced Technology Workshop on Thermal Management Palo Alto, California - USA <a href="http://www.imaps.org/thermal">www.imaps.org/thermal</a>	<a href="mailto:imaps@imaps.org">imaps@imaps.org</a>
10-15-08	10-17-08	7th International Symposium on Microelectronics and Packaging (ISMP 2008) Seoul, Korea <a href="http://www.imapsk.or.kr">www.imapsk.or.kr</a>	<a href="mailto:imapsk@imapsk.or.kr">imapsk@imapsk.or.kr</a>

### NOVEMBER

11-2-08	11-6-08	IMAPS 2008 - Providence Providence, RI <a href="http://www.imaps2008.org">www.imaps2008.org</a>	IMAPS International Symposium <a href="mailto:imaps@imaps.org">imaps@imaps.org</a>
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### DECEMBER

12-15-08	12-18-08	Emerging Microelectronics and Interconnection Technology (EMIT 2008) Bangalore, India <a href="http://www.imaps.org/callfor/emit2008.pdf">www.imaps.org/callfor/emit2008.pdf</a>	<a href="mailto:gramesh@isac.gov.in">gramesh@isac.gov.in</a>
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## 2009

### FEBRUARY

2-25-09	2-27-09	ATW and Tabletop Exhibit on Printed Devices and Applications Orlando, FL <a href="http://www.imaps.org/printed">www.imaps.org/printed</a>	<a href="mailto:jmorris@imaps.org">jmorris@imaps.org</a>
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